EDA: Electronic Design Automation

Luis Mateu
Contents

• What is EDA
• The Phases of IC design
• Opportunities for parallelism
Electronic Design Automation?
The software tools engineers use to design new ICs

If Santiago were as crowded as this chip... ... the streets would be 8 cm. wide!
Main Applications

- Hardware Simulation
- Hardware Compilers
- Place & Route
- Formal Verification
- Mask generation
- Semiconductor Simulation
- etc.
The EDA Industry (not including IP companies)

<table>
<thead>
<tr>
<th>Year</th>
<th>Revenues (in Millions)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY98</td>
<td>$3,000</td>
</tr>
<tr>
<td>CY99</td>
<td>$3,200</td>
</tr>
<tr>
<td>CY00</td>
<td>$3,400</td>
</tr>
<tr>
<td>CY01</td>
<td>$3,600</td>
</tr>
<tr>
<td>CY02</td>
<td>$3,800</td>
</tr>
<tr>
<td>CY03</td>
<td>$4,000</td>
</tr>
<tr>
<td>CY04</td>
<td>$4,200</td>
</tr>
<tr>
<td>CY05</td>
<td>$4,400</td>
</tr>
</tbody>
</table>

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The Cost of Staying in the Game
45 Nanometers Process, 300 Millimeters Wafers

<table>
<thead>
<tr>
<th>Category</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Technology R&amp;D</td>
<td>~$800M/year</td>
</tr>
<tr>
<td>Pilot Line</td>
<td>$1-2B</td>
</tr>
<tr>
<td>Wafer Fab</td>
<td>$3B</td>
</tr>
<tr>
<td>Design</td>
<td>$20-50M</td>
</tr>
<tr>
<td>Masks’ Set (35-40 Masks)</td>
<td>~$8M</td>
</tr>
<tr>
<td>Test (SOC)</td>
<td>Up To 60¢/second</td>
</tr>
</tbody>
</table>

Source: A. Bryant, Intel 2005, IBS 2005, ITRS 2005
## 2005 Worldwide Top 10 Semiconductor Sales Leaders ($M)

<table>
<thead>
<tr>
<th>2005 Rank</th>
<th>2004 Rank</th>
<th>Company</th>
<th>Headquarters</th>
<th>2004 ($M)</th>
<th>2005 ($M)</th>
<th>05/04 % Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Intel</td>
<td>U.S.</td>
<td>$31,430</td>
<td>$35,395</td>
<td>13%</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Samsung</td>
<td>South Korea</td>
<td>$15,830</td>
<td>$17,830</td>
<td>13%</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>TI</td>
<td>U.S.</td>
<td>$10,700</td>
<td>$11,300</td>
<td>6%</td>
</tr>
<tr>
<td>4</td>
<td>7</td>
<td>Toshiba</td>
<td>Japan</td>
<td>$8,589</td>
<td>$9,045</td>
<td>5%</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>ST</td>
<td>Europe</td>
<td>$8,756</td>
<td>$8,870</td>
<td>1%</td>
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<tr>
<td>6</td>
<td>4</td>
<td>Infineon</td>
<td>Europe</td>
<td>$9,180</td>
<td>$8,297</td>
<td>-10%</td>
</tr>
<tr>
<td>7</td>
<td>5</td>
<td>Renesas</td>
<td>Japan</td>
<td>$9,000</td>
<td>$8,266</td>
<td>-8%</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>TSMC*</td>
<td>Taiwan</td>
<td>$7,648</td>
<td>$8,217</td>
<td>7%</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>Sony</td>
<td>Japan</td>
<td>$5,070</td>
<td>$5,845</td>
<td>15%</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>Philips</td>
<td>Europe</td>
<td>$5,692</td>
<td>$5,646</td>
<td>-1%</td>
</tr>
</tbody>
</table>

*Foundry

Source: IC Insights, April 2006
Typical appliances

- Video decoders for DVD players and digital TV
- MP3 decoders/encoders
- Network routing
- Wifi adapters
- ICs for cellular phones
- ICs for digital cameras
- etc.
EDA Players

• Cadence
• **Synopsys**
• Mentor
• Magma

• Software is very expensive
• Just a few customers
• Not robust

• Synopsys installed a R&D center in Chile in June 2006: first EDA R&D center in Latin-America

• 17 engineers and *growing*
Hardware Description Languages

- Verilog
- System Verilog
- VHDL

*They were designed for simulation but they are used for synthesis now*
Characteristics

• Fully parallel
• Everytime you put a + you insert a hardware adder
• * is very expensive
• High level for simulation
• Low level for compiling: not everything can be synthesized
• No floating point
• You specify the width of every datum
• Different kinds of assignment
Phases of IC design

• Design
• RTL coding in Verilog
• Simulation
• Synthesis
• Formal Verification
• Place & Route
• Mask Generation
• Post Silicon Validation
Design

• What the IC is supposed to do
• Input and outputs
Implementation in an HDL: Coding in RTL

```verilog
module counter (input clock, input reset, input enable, output [3:0] counter_out);
wire clock, reset, enable;
always @ (posedge clock) begin : COUNTER
    if (reset == 1'b1) begin
        counter_out <= 4'b0000;
    end
    else if (enable == 1'b1) begin
        counter_out <= counter_out + 1;
    end
end
endmodule
```
Simulation

- Use *timing diagrams*
- Give value to inputs
- Verify that the outputs are correct
Synthesis

- Translate the source program into a circuit
- Equivalent to compiling
- Very time consuming
Formal Verification

• Proves that the output circuit of synthesis is a correct implementation of the source program
• Validates the output of the hardware compiler
• Very time consuming
Place & Route

• Put gates and wires in the chip
• Very time consuming
Mask Generation

- Fracture polygons to trapezoids
- Make optical correction
- Write in a format readable for the fab
- Very time consuming
Post Silicon Validation

• put the IC in a real environment
• simulation is so slow that not everything is tested
• fully test the IC
• some bugs can still show
What the EDA customer wants

- Minimize IC area
- Maximize IC speed
- Minimize IC power
Opportunities for parallelism

• EDA customer may use clusters for:
  ▪ simulation: difficult
  ▪ synthesis: difficult
  ▪ place & route: ?
  ▪ mask generation: yes!

• EDA companies use clusters for:
  ▪ unit tests
  ▪ compiling
  ▪ evaluating quality of results
The Synopsys cluster

- 1200 Opteron processors at 2.4-2.8 GHz
- Network: GigEthernet
- OS: Linux
- Main tool: Platform LSF (load sharing facility)
- In November 2006, Synopsys cluster is ranked number 242 in the TOP500 most powerful computer systems in the world
Conclusions

• Parallelism has just started to appear in EDA
• Difficulty: how to parallelize huge programs
References

- SYNOPSYS (http://www.synopsys.com)
- WORLD OF ASIC (http://www.asic-world.com)
- Platform LSF (http://www.platform.com)