Semantic Multi-View model for Low-Power

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***Abstract*—Power is an important concern in embedded systems. Reduction of power consumption is achieved by balancing the control of multiple domains: switching power, reducing or increasing voltage and changing the frequency on system sections. Model-Driven Engineering gives tools to model the interactions of these domains. In this work, we propose to use MARTE combined to UPF concepts to capture the structure and behavior of these multiple domains. We adopt CCSL to unify the multiform aspects among domains and to verify their proper interaction. We provide an example to illustrate MARTE representation and a simulation of multi-domain power design, specified on CCSL and running on TIMESQUARE tool.**

***Index Terms*—Power Management, UPF, CPF, MARTE, IEEE 1801, CCSL, TimeSquare**

I. INTRODUCTION

Power consumption is a major concern in the design of embedded systems. System on Chips (SoCs) power dissipation has been shown to affect the functionality performances [1]. Additionally, the market trend is to create systems more and more autonomous in energy, such as cell phones and network sensors, which implies straight power consumption constraints on designs.

Existing solutions for energy management mainly focus on two aspects: the management of "clock domains" (such as clock gating or Dynamic Voltage/Frequency Scaling) and the management of "power domains" (like the multi-voltage sections and power switching) [2]. The goal of both aspects is to reduce the electric current consumed during system sleeping state.

The voltage-related entities required for energy management cannot yet be described neither in Hardware Description Languages (HDL, *e.g.,* Verilog, VHDL) nor at more abstract level, where designs focus on the functionality and the structure of the system (like in SystemC and SystemVerilog). Two organizations started an initiative to create a language dedicated to energy management: Accellera with the Unified Power Format (UPF) [3] and Silicon Integration Initiative (SI2) with the Unified Common Format (UCF) [4]. UPF is at the origin of the IEEE 1801 specification [5]. Instead of providing a classical grammar to describe their languages, both UPF and CPF are described by TCL commands. The goal is to use UPF such a language to describe the energy management separately from the system functionality. The major drawback using UPF is the opacity of the TCL commands that are interpreted by proprietary tools to drive some "power-aware simulations" only at the hardware description level. Another restriction of these languages is that they are used only to describe the structure of power domains and not their behavioral impact, which must still be expressed in the same language than the system.

Contrary to the power management, the clock management is usually done in the same language than the system. As a consequence, this aspect is mixed with the functional part of the design.

For an efficient energy management process, it is mandatory to specify clearly the correlation between the power management system, the clock management system and the system function description [6]. To pave the road for such an efficient energy management process, it is important to have a methodological and technological framework able to combine various approaches in order to use the most adequate one depending on the level of abstraction. Using a model-based approach provides the support to combine several models at different abstraction levels [7].

In this paper, we propose to specify the clock management systems, the power management systems and the system architectural description in different views. Our goal is not here to promote the use of aspect modeling or equivalent techniques but instead to understand how these layers can be linked in a semantically clear way. We also aim at providing a modeling framework able to deal with high level power management specification. This paper presents ongoing works and mainly focuses on our experiments on an example described in UML/MARTE. We represent the architecture of a SoC in MARTE at a transactional level. We also use MARTE to define the structure and the behavior of energy management design elements, based on an extraction of the UPF and CPF concepts. Then, we add the description of a crude clock management view. Finally, we use a formal notion of logical time to unify these three views by using CCSL [8].

II. USING MARTETO MODEL OUR VIEWS

MARTE is a UML profile that focuses on the Modeling and Analysis of Real-Time and Embedded systems [9]. In the context of this paper, MARTE provides a component model, hardware resources and a well-defined notion of time making it ideal to model all the views in an homogeneous way.

Due to place restriction, we present only a part of the example used for our experiments[1] (see Fig. 1). In the **architectural view**, we consider two components (a VGA card and a CPU) communicating through a bus.

[1]The whole model is available at http://www-sop.inria.fr/members/Carlos.Gomez_Cardenas/ENCOMAMetamodel.zip

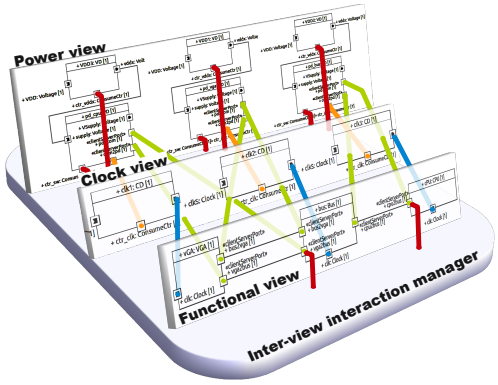

Fig. 1. Example of multi-view in MARTE.

To model the **power view**, we have built a metamodel that gathers the concepts from UPF and CPF[2]. In this view, we describe the hardware resources that control the power delivered to components from the other views. Its main elements are power and voltage domains. These domains are components that control the energy of all components associated with it. To do so, power domain is composed of three kind of elements: power switches, retention cells and isolation cells, which respectively allow turning the module power off, backing up the present state and commanding the restoration of components during the wake-up. Voltage domain is composed by one or multiple power sources that are controlled in order to change the voltage level given to the power domain.

The last aspect that impacts of the power management system is the **clock view**. In Figure 1, this view only represents the clock resources needed to activate the components. However, this view can be more complex and add switches or Phase Lock Loop systems to respectively stop/activate the clocks or to modify their frequency.

Once the domain views is implemented, we need to define the interactions among these views.

III. Inter-view interactions

From our experiments, we have identified two kinds of interactions between views. The first one is just a "connector" concern. It considers data and events exchanged from one view to another. For instance the output of a clock resource in the clock view is connected to the activation port (clock port) of a component in the architectural view. Another example is the association of a component from the clock or architectural views to a specific power domain.

The other kind of interactions is more unusual to deal with and concerns the consistency between the various views used in the design. The consistency is mainly guaranteed by specifying the possible schedules of the events in the system so that the system does not violate any functional or extra functional constraints. Given the views used in the example, this scheduling somehow specifies the energy controller of the system. For instance, in our sketchy example, one can say that the VGA card should be powered on for at least 30 seconds when the CPU request to print something. This simple constraint implies both a causality and a temporal relationship.

To specify such causal and temporal interactions, we use CCSL (the Clock Constraint Specification Language) [8]. CCSL is a formal language dedicated to the manipulation of logical and multiform time. We use CCSL to specify the causal relations between the activation of components in the three views when the system is turned off. We also specify relations between the functional and the power management view to ensure the constraint previously described (*i.e.,* VGA is on for at least seconds 30 when the CPU is printing).

CCSL has a formal semantics that can be exploited to detect invalid specifications (*e.g.,* deadlocks) or to compute a correct execution (by simulation), if any, in the TimeSquare tool[3]. We have developed the tool TimeSquare specifically to analyze MARTE and CCSL models. Consequently, we have a first feedback about the interactions between the views (see Fig. 2 for a simple example).

IV. Conclusion and future works

In this paper, we report our study on the modeling of the energy management system using multiple views. The main goal is to study the interactions between these views. We use MARTE to describe the various views but we have based the power view on a metamodel dedicated to power management inspired from the IEEE 1801. We have just used MARTE as a graphical environment to model the energy management concepts. To specify the interactions between the views formally, we use the notions of logical and multiform time brought by CCSL. By doing so, we can check the consistency of the interactions by using our tool called TimeSquare.

The experiments look promising and several future works are possible. In a close future, our goal is to show the importance of the multi-view interactions for the safe introduction of extra-functional concerns from the first steps of the development process. Future works also include extending our metamodel to model Retention Cells and Level Shifters that are essential to the power management system. We believe that this structural metamodel connected to a behavioral metamodel can help verifying the correct sequence that is to be implemented on power-aware designs. In addition, the metamodel can be enriched with power units to perform a quantitative analysis of the system power consumption.

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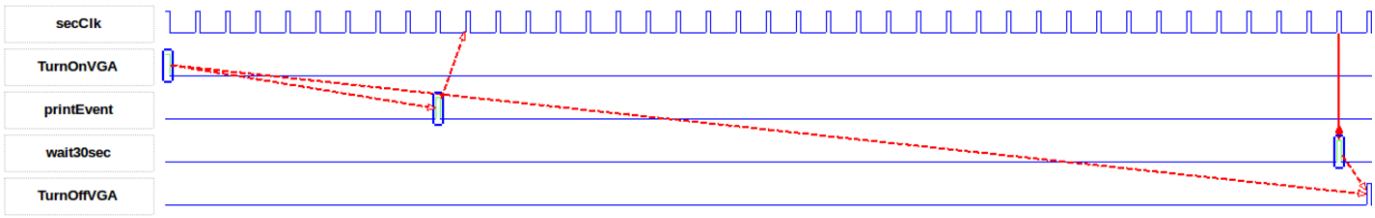

Fig. 2. Simulation of an interaction between views specified in CCSL.

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