Implementation of a Multi-Channel Baseband CDMA Receiver on a ADSP2189M Processor

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Abstract **-** The origins of Spread spectrum are in military field and navigation systems. Techniques developed to provide efficient data communication proved for CDMA mobile technology. To meet data communication requirements for commercial mobile standards like GSM, implementation of a multi-channel CDMA receiver offering a data rate of 9600 bps is illustrated. The CDMA receiver consists of a Soft Correlator, Acquisition & Synchronization algorithms and Data Extractor. This paper presents a brief overview of CDMA receiver, mathematical model, and functional block diagram with implementation details and its results. The features of ADSP2189M processor, in relevance to the CDMA receiver implementation, like Serial ports, General-purpose flags, Timer, BDMA mode and multi-instruction in single cycle, are highlighted.

Index terms: Code Division Multiple Access, Synchronization, Memory, MIPS

I. Introduction

Direct sequence spread spectrum techniques based on BPSK modulation have received considerable attention from both military & commercial mobile communication systems. For data communication applications, 9600 bps baseband multi-channel CDMA receiver is implemented on ADSP2189M platform. This receiver reliably extracts data for SNR greater than –5 dB. Acquisition algorithm facilitates both cold and warm acquisition. The acquisition time is of the order of msec. Synchronization loops for receiver dynamics are implemented. The receiver has effective algorithms to declare track fail based on signal and noise powers.

The ADSP2189M is a single chip microcomputer optimized for DSP and other high-speed numeric processing applications [1]. It is a 16-bit fixed-point processor with independent ALU, Multiplier/Accumulator and a Barrel shifter. It has 192K bytes of RAM configured as 32K words of on-chip program memory RAM and 48K words of on-chip data memory RAM. It has 66 MIPS with sustained performance.

The first few sections explain CDMA concepts, mathematical analysis and implementation of the receiver on the ADSP 2189M processor. The later sections talk about the performance results of the receiver. ADSP2189M features in relevance to the receiver design are highlighted. The features of implemented receiver are listed. Conclusions are made in the last section.

II. Receiver Description

A. CDMA concepts

CDMA users are uniquely identified by a code sequence embedded as an address within the carrier waveform, which gives the receiver the capability of selective addressing. To recover a signal, the receiver correlates the sum of incoming signals against address sequences. This process maximizes the output for the signal matching the address sequence. However the receiver must have the knowledge of the address sequence. Therefore, address coding provides communication privacy [2].

To achieve isolation between CDMA users, it is necessary to select code sequences with properties by which a correlation process would build up the signal of the matching sequence while maintaining the low correlation values for non-matching sequences. Gold code sequences have a bound on the cross correlation values for any pair of sequences, taken over the full sequence period. Furthermore a single Gold code set can produce a large number of sequences that take on uniformly low-cross correlation values. Such properties make Gold codes attractive for CDMA applications.

Gold code sequences have a period of 2^m-1, where m is the length of shift register used to generate the Gold code. The cross-correlation value of two such sequences are no larger than $2^{\{(m+2)/2\}}$+1. From a single Gold code generator, we can produce a total of 2^m +1 new sequences. A particular code is chosen to modulate data for a particular channel and the modulated is extracted using the same code at the receiver.

Acquisition algorithms are used to acquire a particular channel, where in the code and frequency ambiguity about the multiplexed signal is resolved. Synchronization algorithms are used to maintain the receiver synchronization with the incoming signal.

B. Mathematical model

The multi-channel DSSS-BPSK modulated baseband signal is

$$s(t) = \sum_{k=-\infty}^{\infty} \sum_{m=1}^{M} \sum_{i=0}^{N-1} d_m(k) c_m(i) \cos(w_c t + \theta) + n(t) \quad (1)$$

$d_m(k)$ is the kth-input data bit from the mth channel

$c_m(i)$ is the chip from the mth spreading sequence

n(t) is the Additive White Gaussian Noise.

To detect the data, the code and the carrier should be removed.

mth user data will be recovered using the mth spreading sequence.

For m=1, the despreaded signal is given by Equation (2).

$$s_d(t) = \sum_{k=-\infty}^{\infty} d_1(k) \cos(w_c t + \theta) + \sum_{k=-\infty}^{\infty} \sum_{m=2}^{M} \sum_{i=0}^{N-1} d_m(k) c_m(i) c_1(i) \cos(w_c t + \theta) + n(t) c_1(t) \quad (2)$$

In Equation (2), second term on the right hand side gives the cross correlation term.

Gold codes give very low cross correlation, and hence the second term has negligible effect. Due to this cross correlation term the number of channels supported by the CDMA system will be limited. The cross correlation term depends on the code sequence length used for spreading.

The noise term in equation (2) will not be effected in the required band.

Equation (2) can be approximated as below

$$s_d(t) = d_1(t) \cos(w_c t + \theta_1) + n(t)\, c_1(t) \quad (3)$$

θ_1 can be recovered using FLL / PLL by which the data can be detected. The order of FLL or PLL depends on the dynamics of receiver. The current design uses a 3rd order FLL.

The 3rd order FLL equations are given below [3].

$$f''_{k+1} = f''_k + W_n^{\,3}.T\, fe_k \quad (4)$$

$$f'_{k+1} = f'_k + T.\, f''_k + 2\, W_n^{\,2}.T\, fe_k \quad (5)$$

$$f_{k+1} = f_k + T.\, f'_k + 2.W_n.T.\, fe_k \quad (6)$$

where fe_k is the frequency error at instant k and f_k is the frequency correction factor, T is the sample period, and W_n is 1.2 times the filter bandwidth.

Similarly for m^{th} channel, the reference code will be $c_m(t)$. The same analysis is applied for the m^{th} channel to demodulate the data.

III. Implementation

ADSP2189M processor has a key role in the implementation of the receiver. It is interfaced to other peripherals like FLASH memory, UART and EPLD for communicating purposes.

The Fig. 1 and Fig. 2 shows all the functional components of the CDMA receiver.

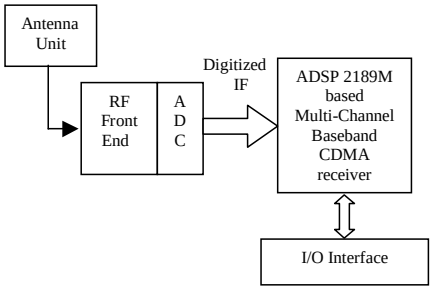

Fig. 1 Interfacing diagram for Multi- Channel Baseband CDMA receiver

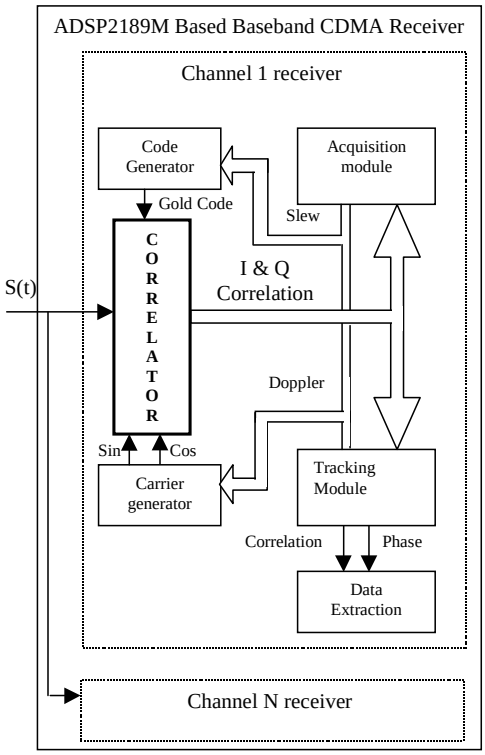

Fig. 2 Functional diagram of ADSP2189M based Multi channel CDMA Baseband receiver

The following modules are realized in software for ADSP2189M.

A. Code generator

This module generates the Gold code for despreading with the help of aid from the I/O interface. This enables online programming of codes for Multi-channel baseband CDMA receiver. During tracking, the code generator interprets the code phase corrections for despreading to maintain synchronization. This is completely implemented in software.

B. Carrier Generator

This module will generate the required carrier frequency with phase continuity. It generates both Inphase and Quadriphase carriers for demodulation. During tracking, this module incorporates the carrier corrections computed by carrier synchronization loops.

C. Correlator

This module despreads the incoming signal and removes the residual doppler. It consists of multipliers & filters. It is aided by the doppler & spreading code input from the acquisition & tracking modules explained in the following sections.

D. Acquisition

This module performs two-dimensional search for time & frequency ambiguity in the incoming signal. It consists of Cold start acquisition, Warm start acquisition and Reacquisition modes. In the absence of doppler aid, Cold start acquisition module performs search. Incase the doppler aid is available with an accuracy of 2.4 KHz, Warm start acquisition is activated. Reacquisition is performed incase the receiver loses track due to the minor signal failures.

Cold start acquisition algorithm takes a time of < 2 sec to do the complete time and frequency search. Warm start acquisition algorithm, which works on aid, takes a time of < 185 msec. Reacquisition algorithm, which works during signal failures of minor duration, takes a time of < 50 msec.

E. Tracking

To maintain the synchronization with the incoming signal against the carrier doppler & code doppler due to the dynamics of the receiver, tracking software is implemented. Vehicle dynamics mentioned in section VI call for a 3^{rd} order FLL & 3^{rd} order delay lock loop to maintain synchronization. It also aids in extracting the data when it is in lock with the incoming signal. Incase of low SNR's or signal failures the tracking software declares the fail.

Tracking software has Convergence, Sideband detection and Data Extraction algorithms. Convergence algorithm work towards minimizing the doppler errors so that the receiver is fine-tuned. Sideband detection algorithm works to filter the side bands of the correct doppler. Data Extraction algorithm works on the phase outputs of the carrier lock loop to extract data.

Flag updation for I/O interface, aid updation for Reacquisition algorithms are also a part of tracking software.

F. HCOMM software

Host communication software, which supports GUI, is also developed on ADSP 2189M platform. This enables the user to observe the receiver performance. The user can program the receiver parameters like doppler, CDMA code aid etc. to monitor the receiver performance under different environments. This helps the developer to develop, and test the software efficiency.

All the above modules are implemented in software. Since the correlator is a MIPS consuming function, it is coded in assembly. All of acquisition and synchronization modules are implemented in C for more flexibility and ease of upgradation.

For testing purposes, the receiver is implemented for 2 channels. The complete receiver software consumes 48 MIPS. The total program memory used is 6.2 Kbytes and the data memory used is 7.8 Kbytes.

IV Results

This section gives the acquisition & tracking results of the implemented system. Data outputs from both the channels are compared with the transmitted data in the following plots.

A. Acquisition results

The acquisition performance of the receiver is shown in Fig. 3. In CDMA signal simulator, the signal is generated such that the output is having 0 KHz Doppler & Chip number is 83. The search results in Frequency & times are shown in the following plots.

The first figure shows one frequency search results. This follows sinc behavior with frequency. The second figure shows time search results. This follows a triangular behavior with time.

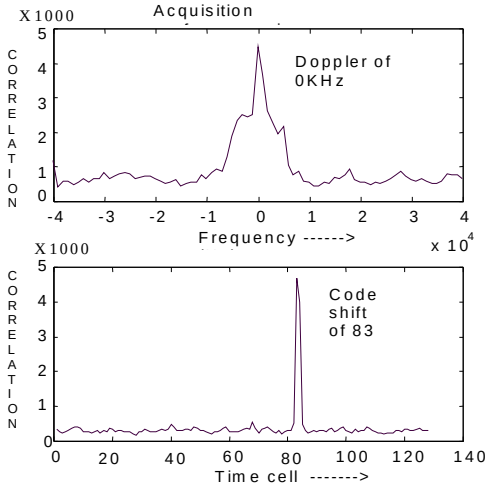

Fig.3 Acquisition algorithm performance in both Frequency and Time domain

B. Tracking Results

1) Carrier lock loop

Carrier lock loop consists of 3rd order FLL to track the doppler drifts.

Tracking is a sequence of three states, Convergence, Side band detection and Data Extraction. In Convergence State, the doppler tries to converge to the actual doppler or to the side bands of 4.8 KHz about the actual doppler. Fig. 4 shows the performance of Carrier filter with 1 KHz initial error.

Side band detection module eliminates the side bands and then enters into Data Extraction mode. During Data Extraction State, the tracking loop tracks the actual doppler and extracts the data. Fig. 5 shows the doppler behavior during tracking. The actual simulated doppler is 10 KHz. The acquisition loop resulted in a doppler of 6 KHz with an error of 4 KHz. In tracking, the doppler converged to 5.2 KHz and Side Band Detection algorithm detected the actual doppler 10 KHz which is 4.8 KHz away from 5.2 KHz. Then the control is passed to the Data Extraction module where the tracking loops track the 10 KHz doppler and extract the data.

2) Code lock loop

Code lock loop consists of a 3rd order delay lock loop to track the code drifts.

Due to sample clock drifts and dynamics of the receiver, the chips in a data bit will not be uniform resulting in a code drift. Code lock loop consists of phase detector to compute code phase. Code filter is implemented on this raw code phase. This filter smoothens the code phase. Whenever the code phase changes by 180^o correction to code chip is applied. Results are given for both positive and negative code dopplers. In the Fig. 6, a phase change of 180^o ($+90^o$ to -90^o) has occurred for a duration of 0.12 sec indicating a negative code doppler of 8.33Hz.

Similarly, in the Fig. 7, phase change of 180^o (-90^o to $+90^{o)}$ has occurred for a duration of 0.14 sec indicating a positive code doppler of 7.11Hz.

3) Performance against SNR variations

Correlation values are measured with different SNRs for both 1– bit and 4– bit processing.

The following is the analysis for 1-bit and 4-bit with 1-channel and 2- channel data input

Fig. 8 shows the correlation values for 1-bit processing.

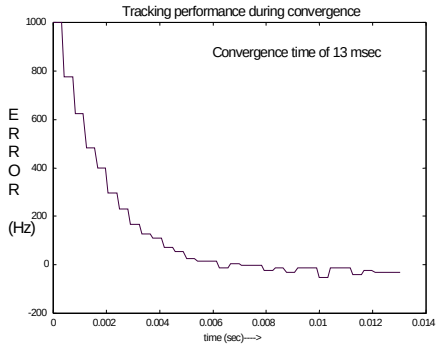

Fig.4 Carrier Lock Loop filter performance during Convergence

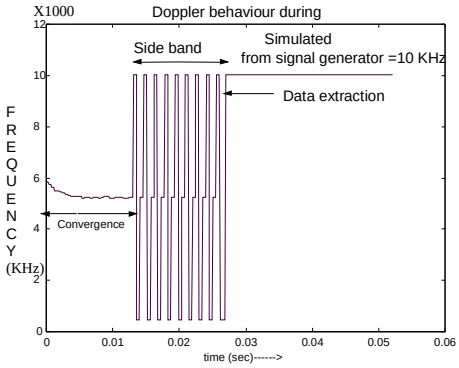

Fig.5 Performance of Sideband detection and Data Extraction algorithms

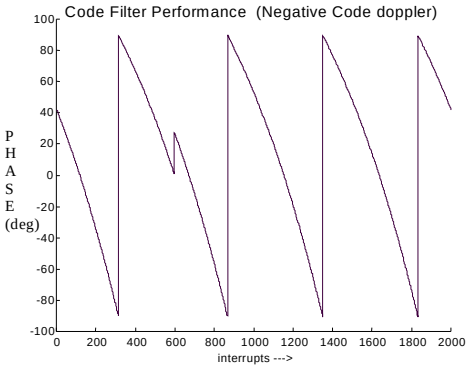

Fig.6 Delay Lock Loop code filter performance for a negative code doppler of 8.33 Hz. Code phase integrated for 3 interrupts

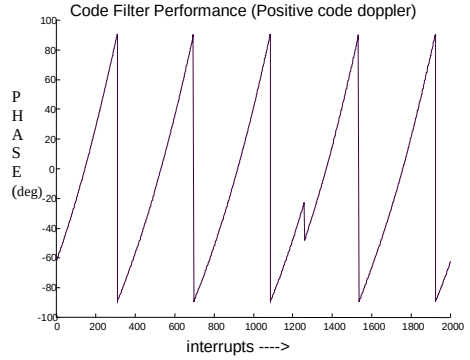

Fig. 7 Delay Lock Loop code filter performance for a positive code doppler of 7.11 Hz. Code phase integrated for 3 interrupts

Saturated values of 23.34 dB in case of 1–channel and a value of 22.14 dB in case of 2-channels are observed. A value of 23.94 dB is observed for an SNR of ∞.

Fig. 9 shows correlation values for 4-bit processing. In 4-bit processing one sign bit and three magnitude bits are considered. A saturated value of 36.45 dB in case of 1–channel and a value of 35.95 dB in case of 2- channels is observed.

In 4-bit processing the correlation values are scaled up by 13 dB approximately. It depends on the levels of the local signal, incoming signal and the doppler frequency.

In both the Fig. 8 and Fig. 9, the correlation loss due to the cross correlation of the second channel is around 1.2 dB.

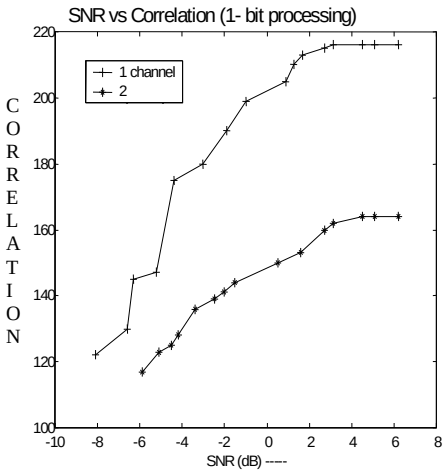

Fig. 8 Correlation variations against SNR Variations. To observe the performance in presence of two channels, one-channel results also observed. Only sign bit is considered for processing

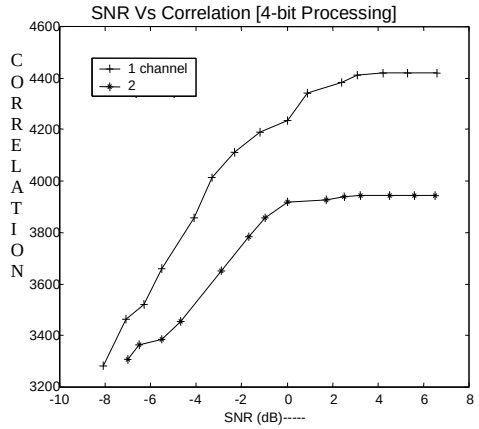

Fig. 9 Correlation variations against SNR Variation incase of 4-bit processing.

Fig. 10 shows the BER variations for 1-bit and 4-bit processing. Incase of 4-bit processing zero errors are observed from –6.2 dB to positive side.

Incase of multi-bit processing the incoming signal is approximated as a sinusoid. Inside the receiver, multi-bit carrier generator is provided for carrier demodulation. In multi-bit case the resolution is higher and the phase measurements are comparatively good for low signal to noise ratios [5]. The Data Extraction works optimally in multi-bit processing there by optimal BER is achieved.

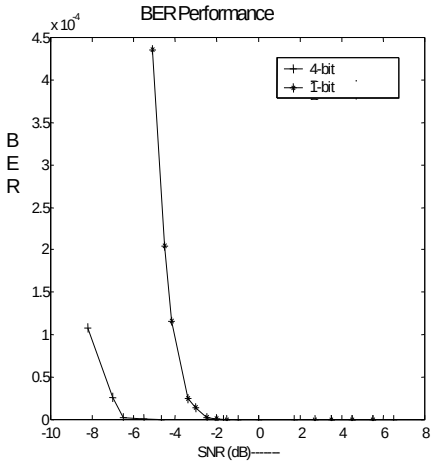

Fig. 10 BER measurement for different SNR's. Both 1-bit & 4-bit processing is considered.

V. ADSP2189M Features used in CDMA Receiver Design

The features of ADSP2189M, which made the implementation of Multi-Channel Baseband CDMA receiver simpler and easier, are illustrated below [4].

A. Serial Port as utilized in the current design is given below

i. Word Length: Each SPORT supports serial data word lengths from 3 to 16 bits which made multi – bit correlator possible.

ii. Autobuffering : Using the DAGs, each SPORT can automatically receive an entire circular buffer of data with an overhead of only one cycle per data word. This feature enables collection of input data in the background, while the core is involved in processing.

iii. Interrupts: Each SPORT section generates an interrupt after transferring an entire buffer in autobuffering mode. The time between two interrupts is used in the determination of processing time for data bits.

B. Timer generates time information based on processor's cycle time. This timing information is used in many aspects of receiver which are listed below

i. To measure signal acquisition time

ii. To transfer control to time-based modules

iii.To profile all the modules of the receiver

C. General Purpose I/O Flags provide flexible system signaling. In the current design the flags are used for the following

i. To output demodulated data
ii. To provide data clock
iii.To provide doppler status
iv.To provide channel status (Acquisition, Tracking and Data Extraction)
v. To provide input to the Reset circuitry

D. 3-Bus Architecture allows dual operand fetches in every Instruction cycle. This enables multifunction instructions to be executed in the same cycle. This feature is used extensively in our receiver software thereby achieving maximum throughput.

E. 66 MIPS of ADSP2189M provide 6875 cycles for a data rate of 9600 bps. The 2–channel CDMA receiver is implemented in 5000 cycles which is equivalent to 48 MIPS with some additional features. Present design has spare MIPS to implement additional features like Viterbi FEC decoding and Data base manager etc.

F. BDMA supports booting from external FLASH memory. This feature provides flexible upgradation of software. At reset the Byte Memory Select signal is used for booting from external FLASH. This eliminates the necessity of using external logic for booting.

G. Emulation mode of ADSP2189M has on – chip emulation support and an ICE – port, a special set of pins that interface to the EZ – ICE.

H. I/O Space memory interface with 2K locations supports multiple peripherals. In our application, UART, BUFFERS and LATCHES have been interfaced in I/O space. Host communication software uses UART. Buffers and latches are used for data interface.

VI Features of ADSP2189M based baseband CDMA receiver

The features of ADSP2189M based Multi-channel CDMA baseband receiver is illustrated below.

- ADSP2189M DSP based software solution
- Standard Data rate of 9600 bps
- Chipping rate of 1.2192 MHz
- Multi-channel Soft correlator
- Programmable carrier generator
- Programmable code generator
- Multi-Channel Data extractor
- Programmable filters for reliable code and carrier tracking
- Acquisition time of less than 2 sec in absence of Doppler aid
- Acquisition time of less than 185 msec in presence of Doppler aid
- Reacquisition of the signal within 50 msec
- BER of $1x10^{-6}$ with an SNR of –5 dB
- Reliable performance for the dynamics of commercial standard receiver
- PC based Graphical User Interface
- In-circuit FLASH programming for software upgrade.

VII Conclusions

In this paper we have presented an ADSP2189M based design of Multi-Channel Baseband CDMA receiver. The mathematical model and block diagram is illustrated. The results of implemented design are given. ADSP 2189M processor features in relevance to our design are elaborated. The features of our current version CDMA receiver are listed out.. Our current research includes increasing the number of channels & higher data rates for efficient data communication in ADSP219X family processors.

VIII Glossary

CDMA	Code Division Multiple Access
DSSS	Direct Sequence Spread Spectrum
BPSK	Binary Phase Shift Keying
BER	Bit Error Rate
SNR	Signal to Noise Ratio
HCOMM	Host Communication

IX Acknowledgements

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X References:

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