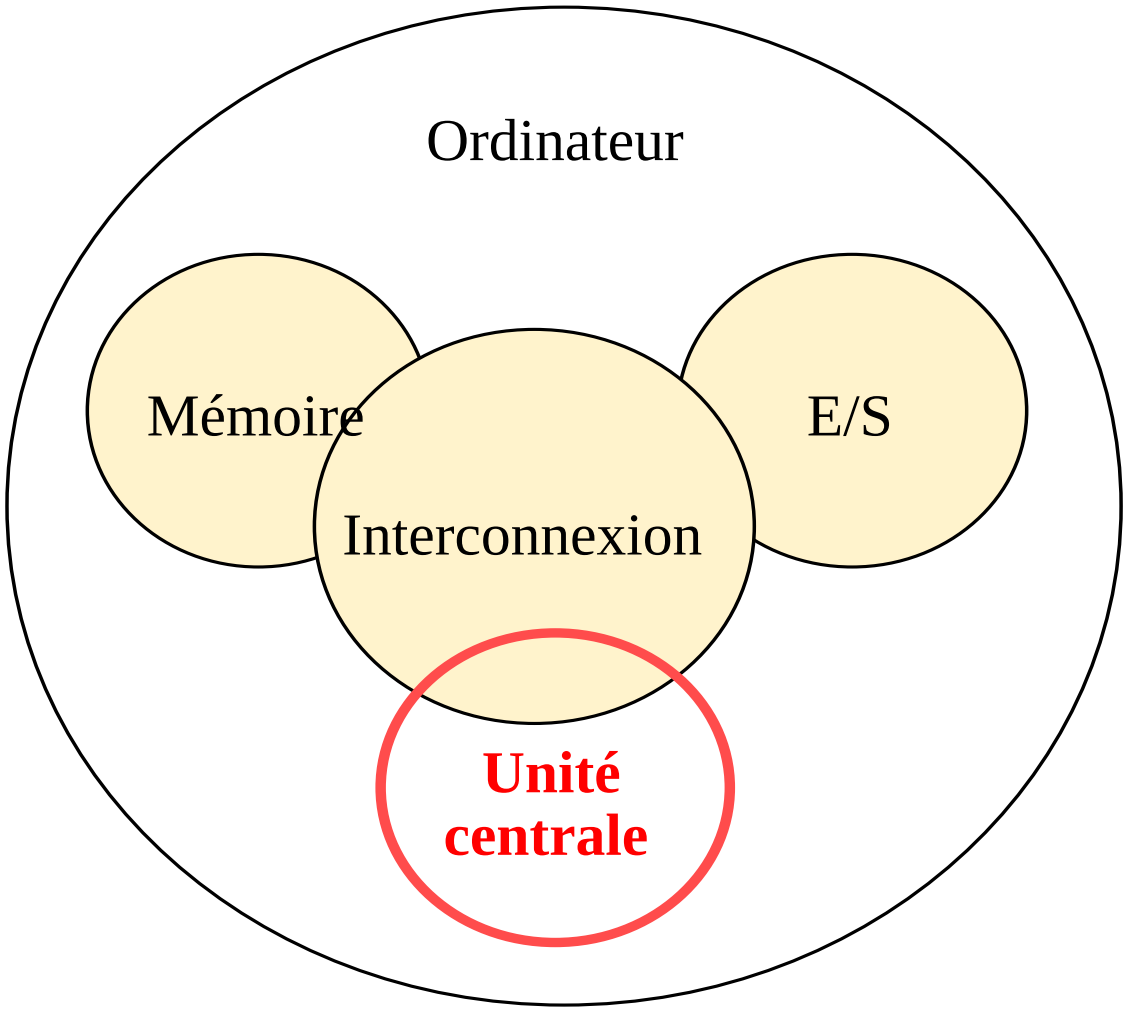
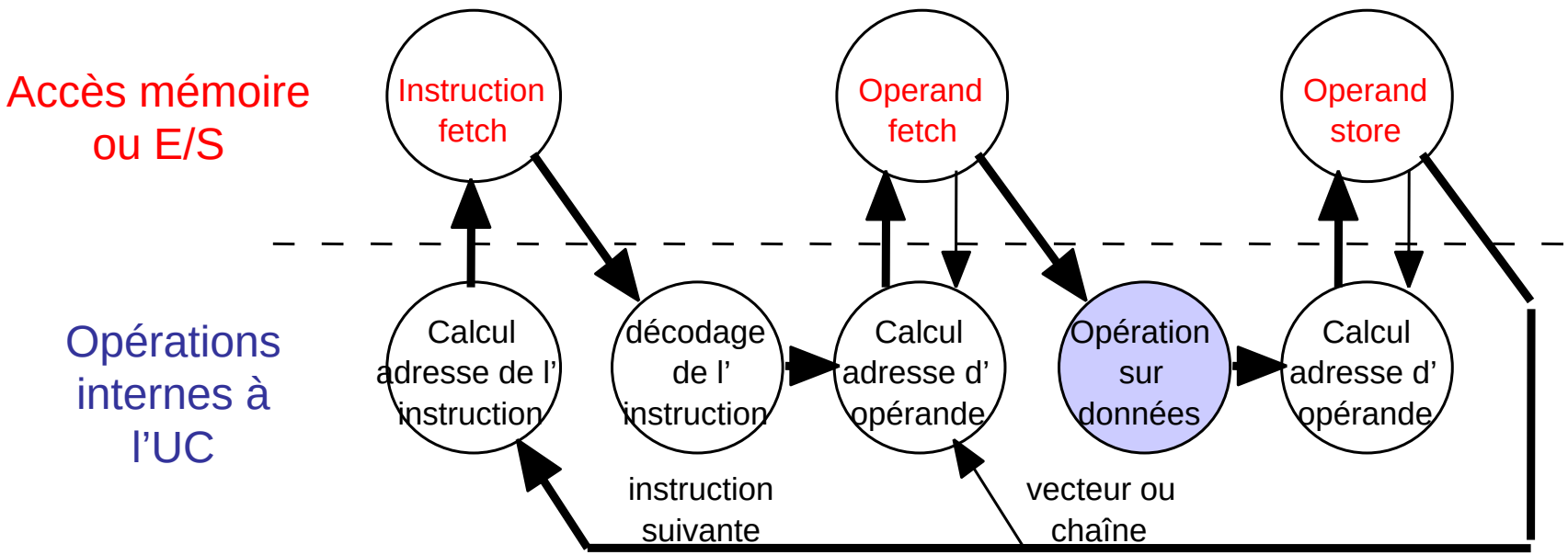
Central Processing Unit

CPU

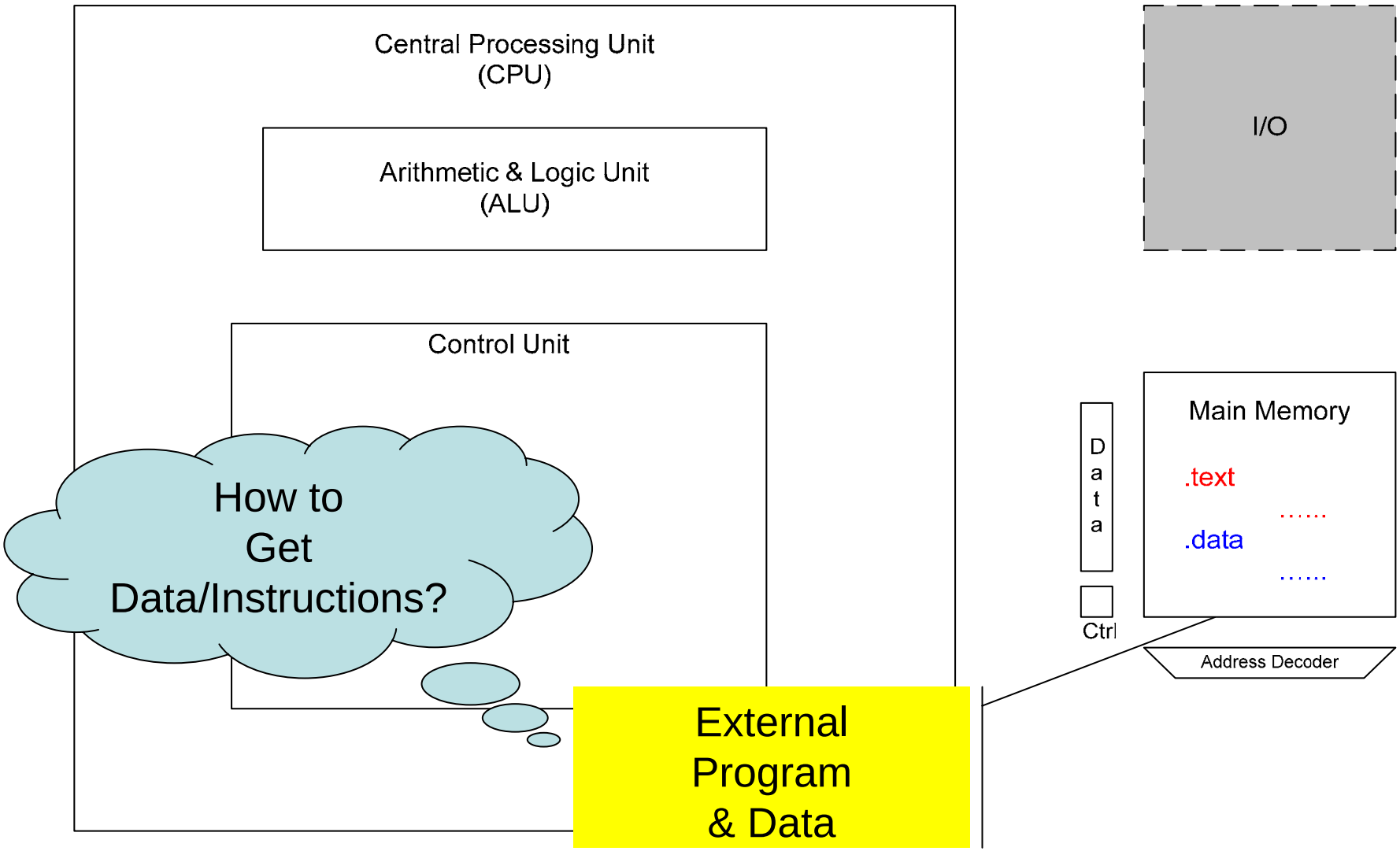
Central Processing Unit



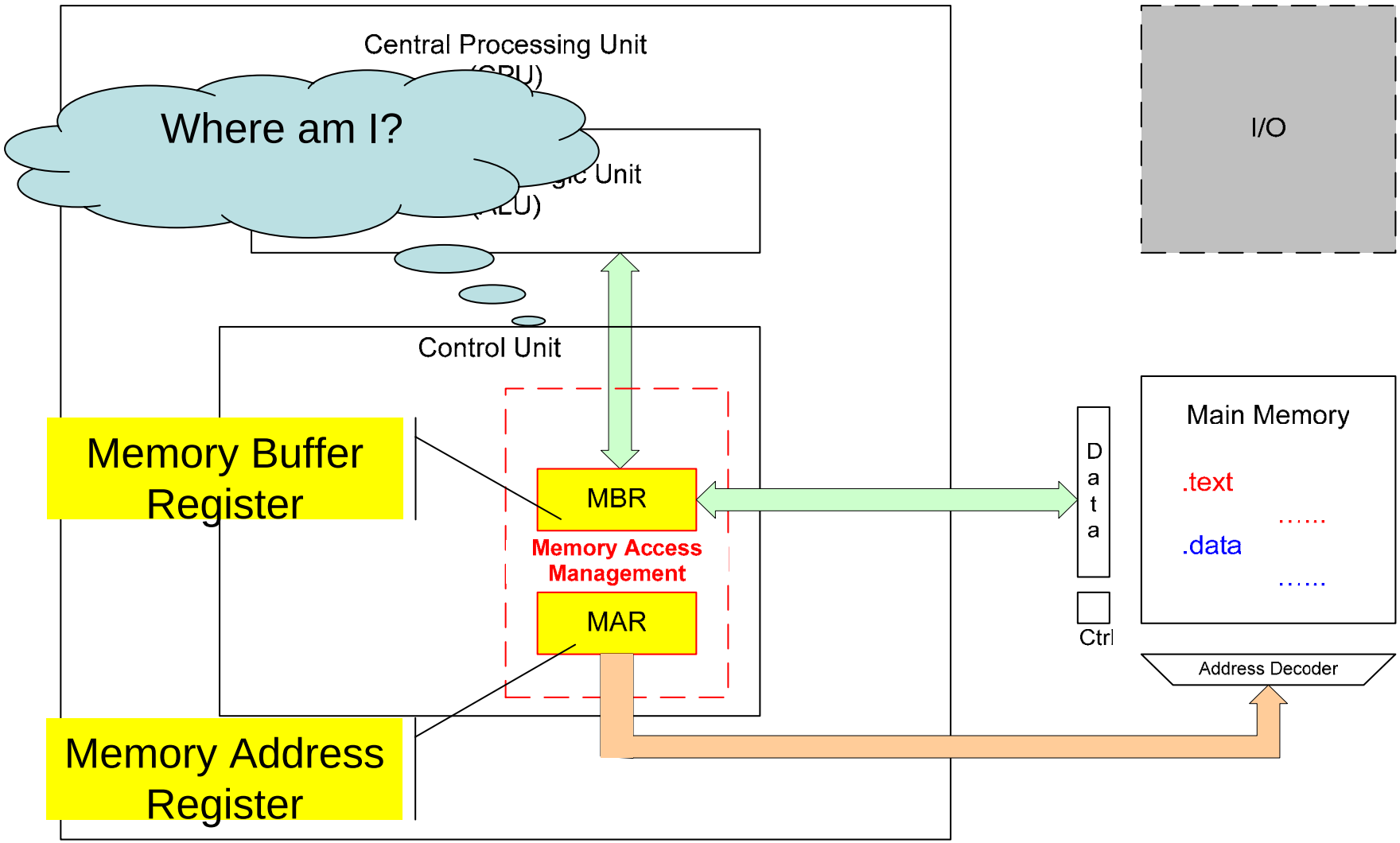
Instruction Cycle



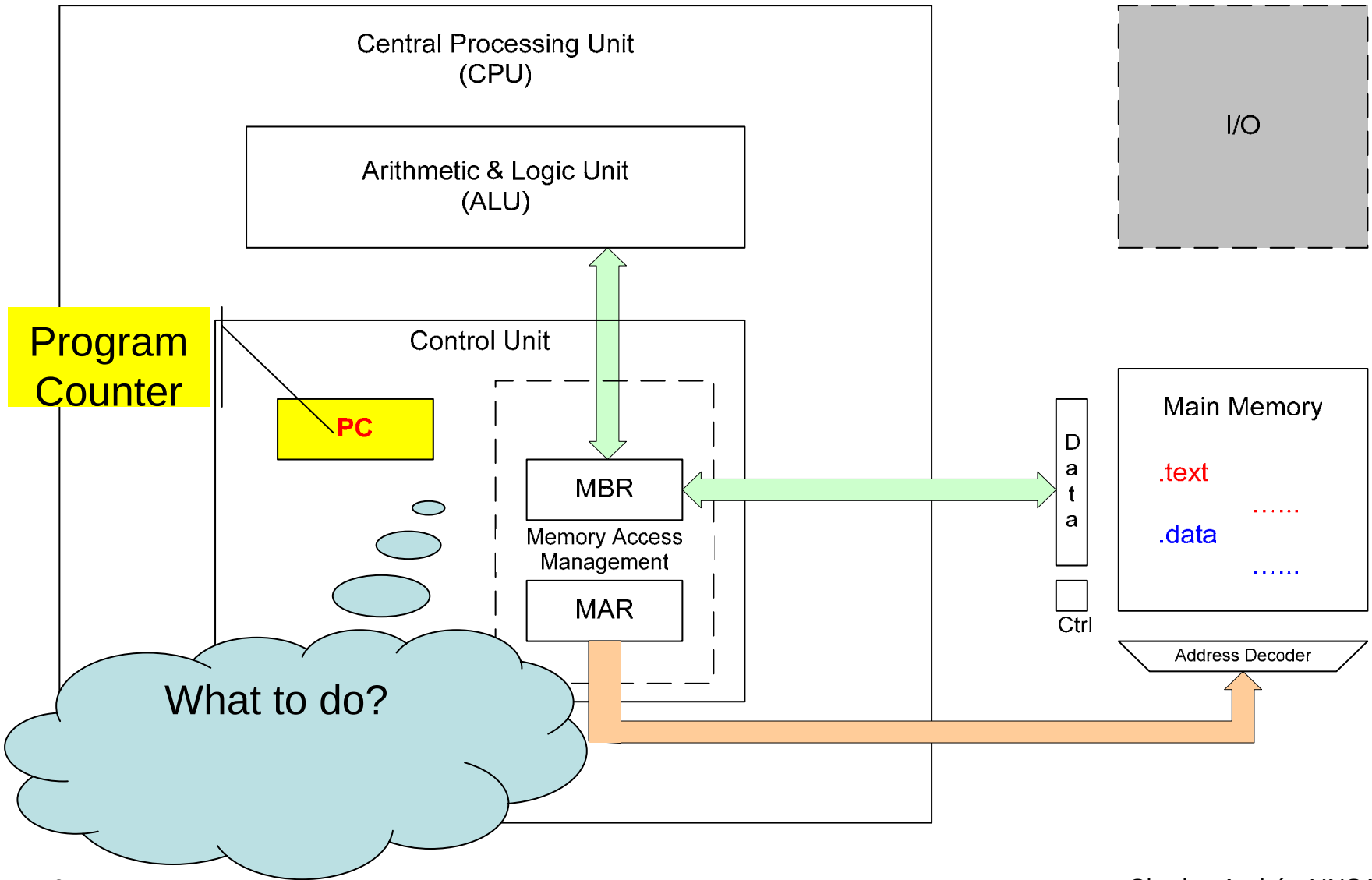
Central Processing Unit



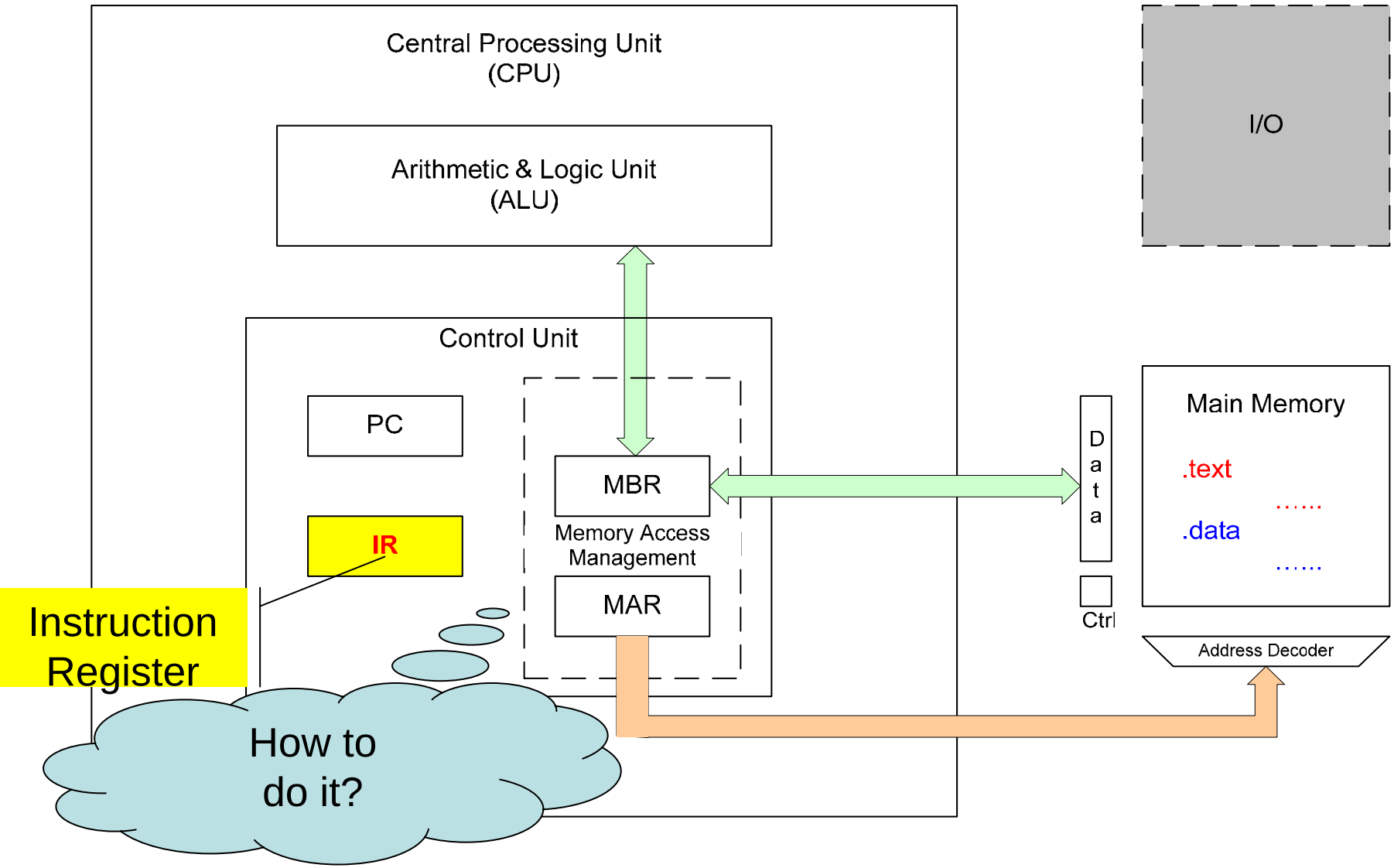
Central Processing Unit



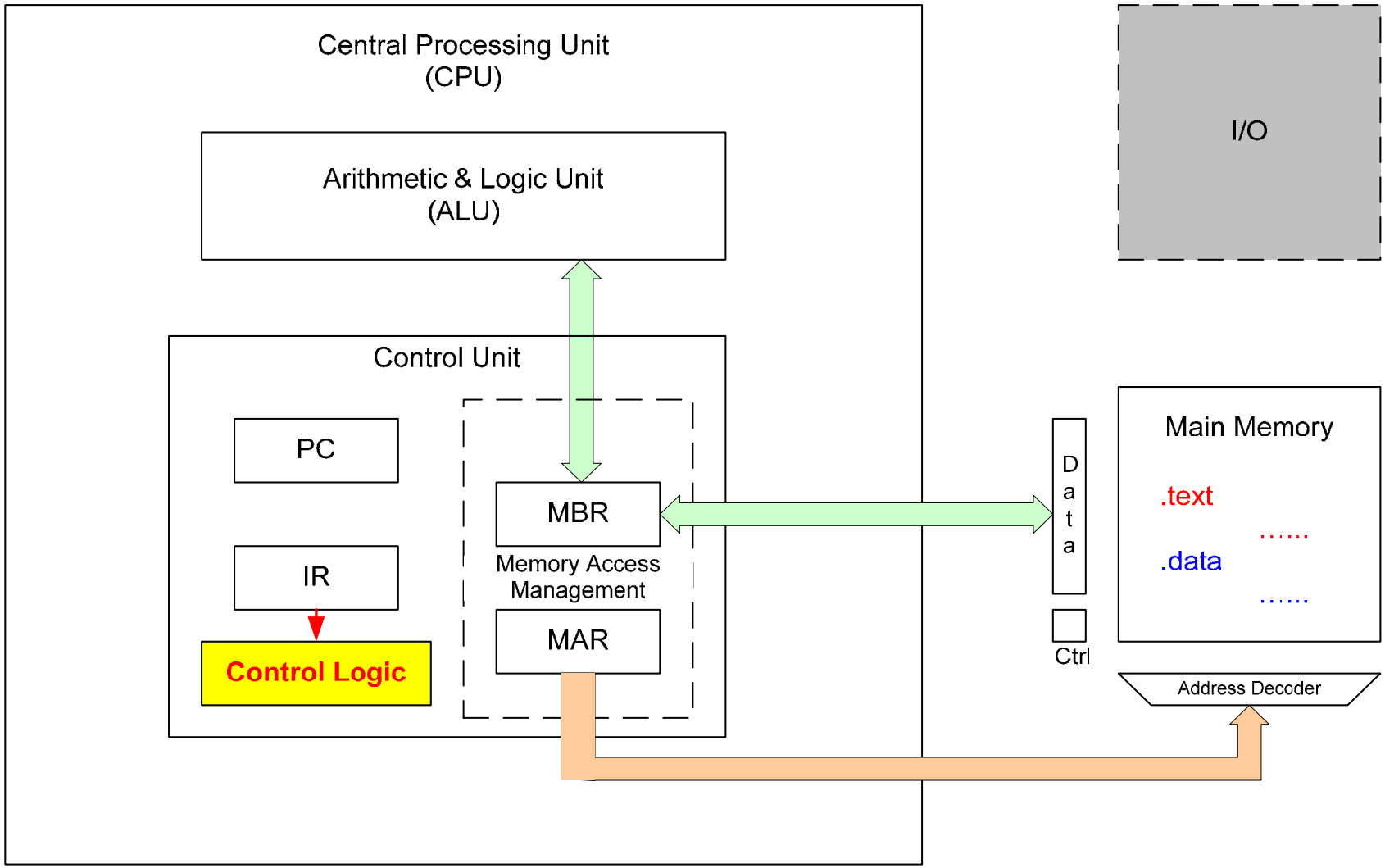
Central Processing Unit



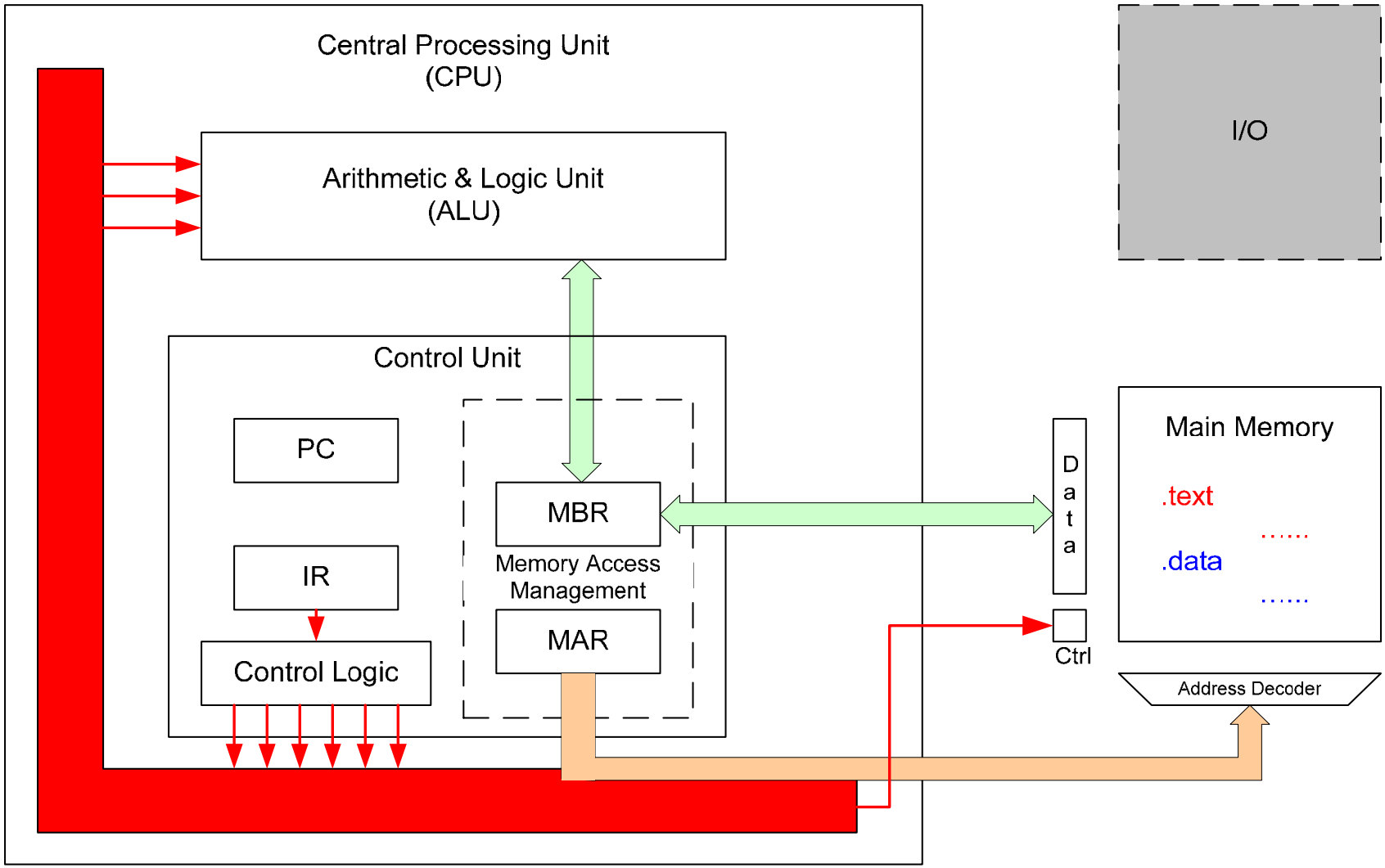
Central Processing Unit



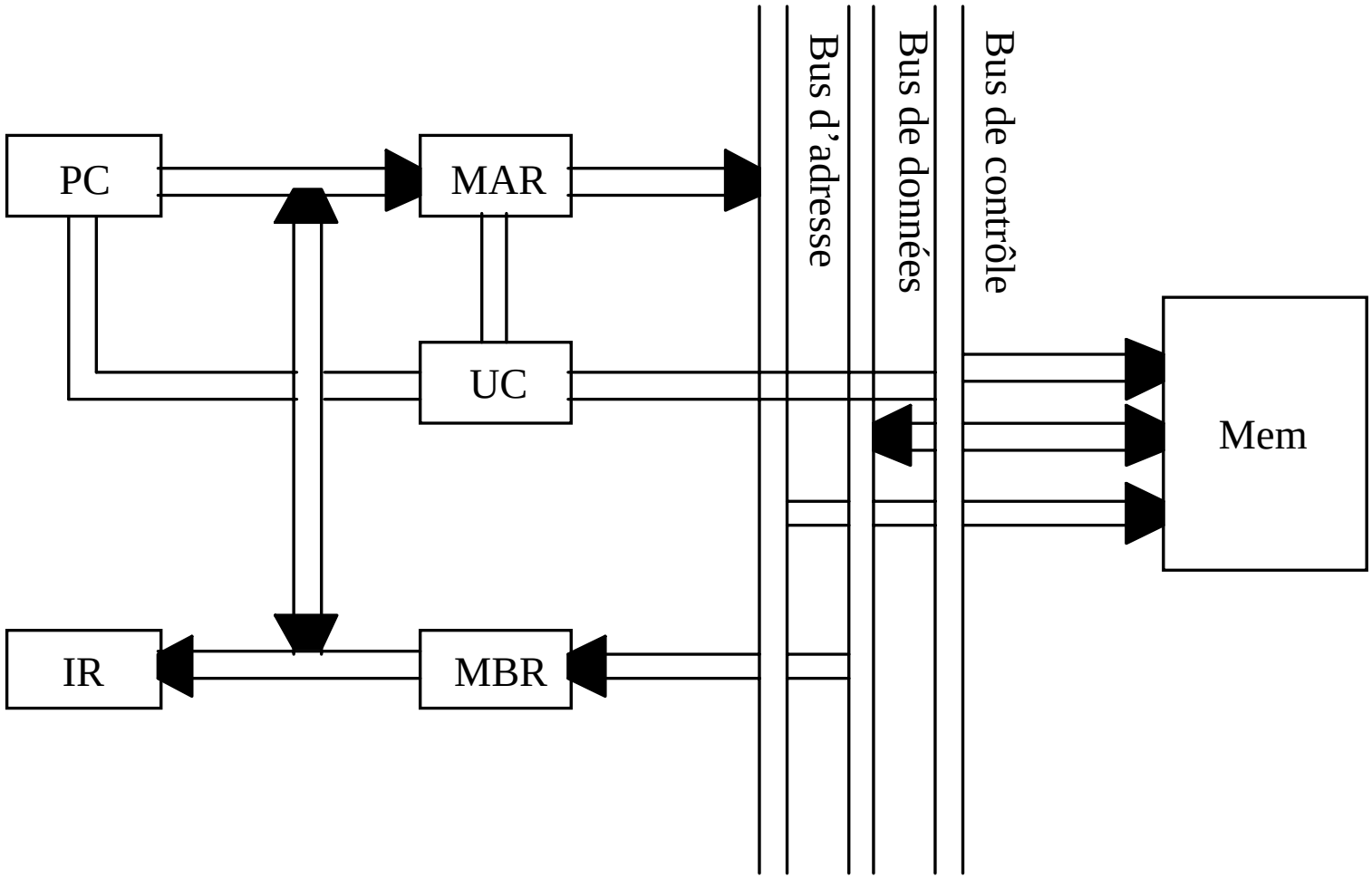
Central Processing Unit



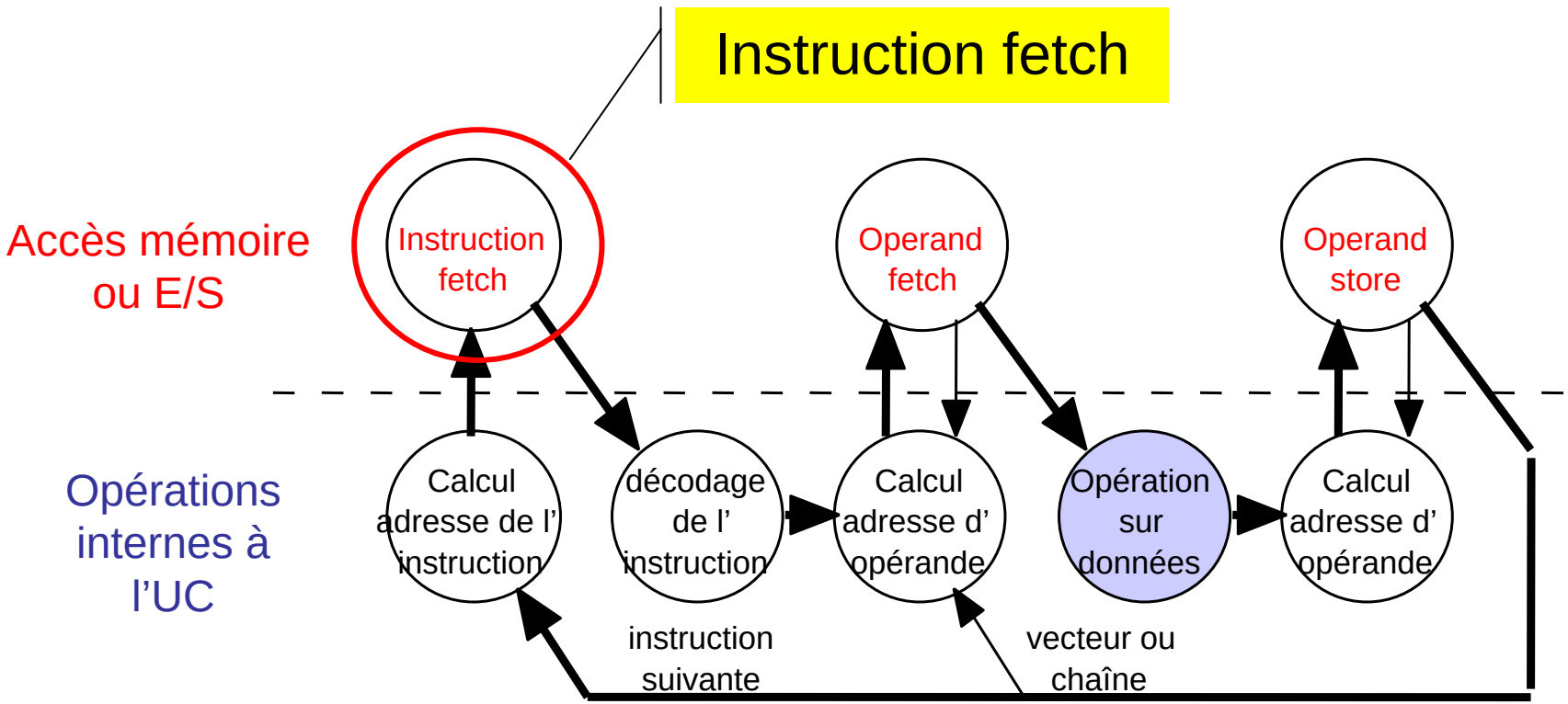
Central Processing Unit



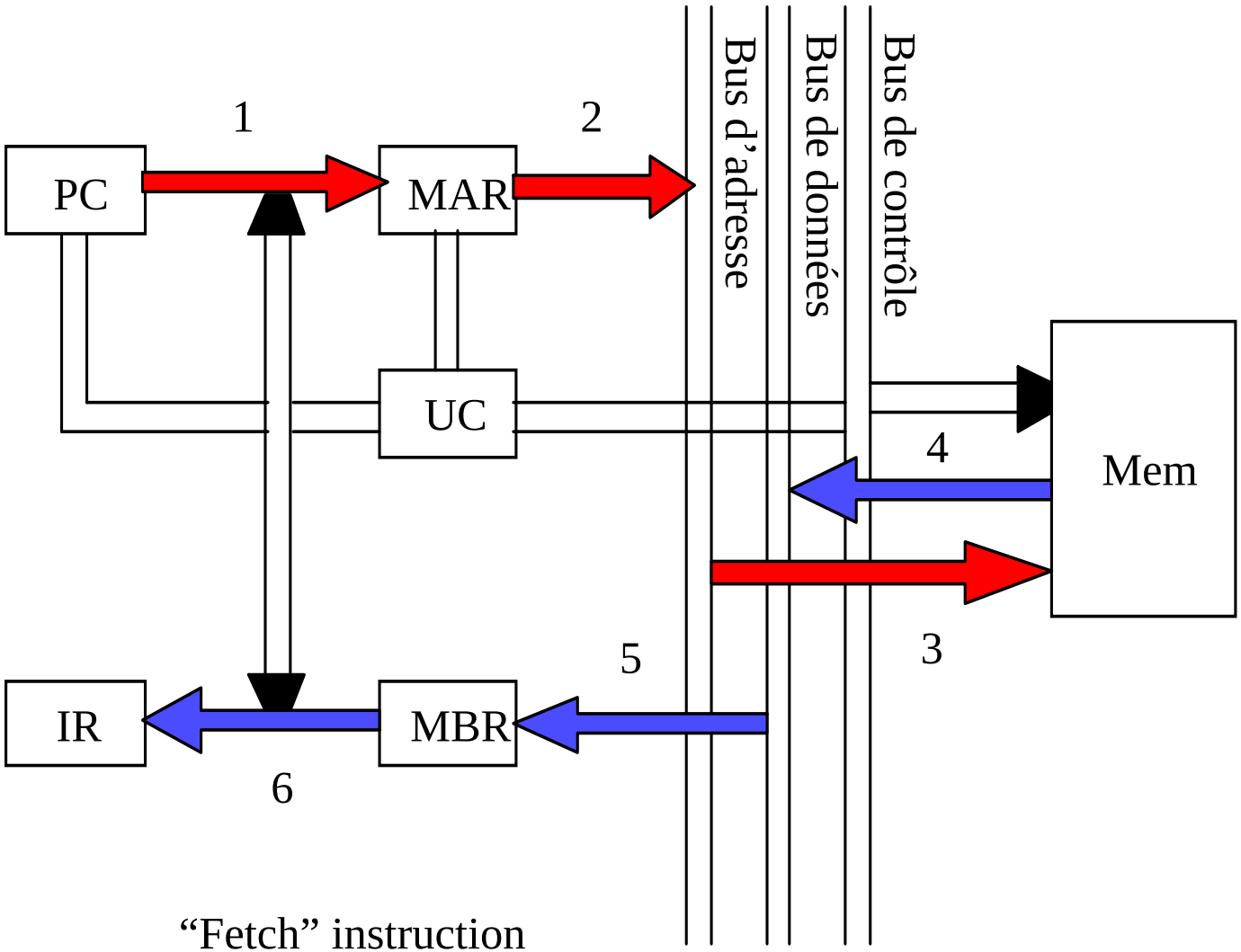
Data / Control Paths



Instruction Cycle

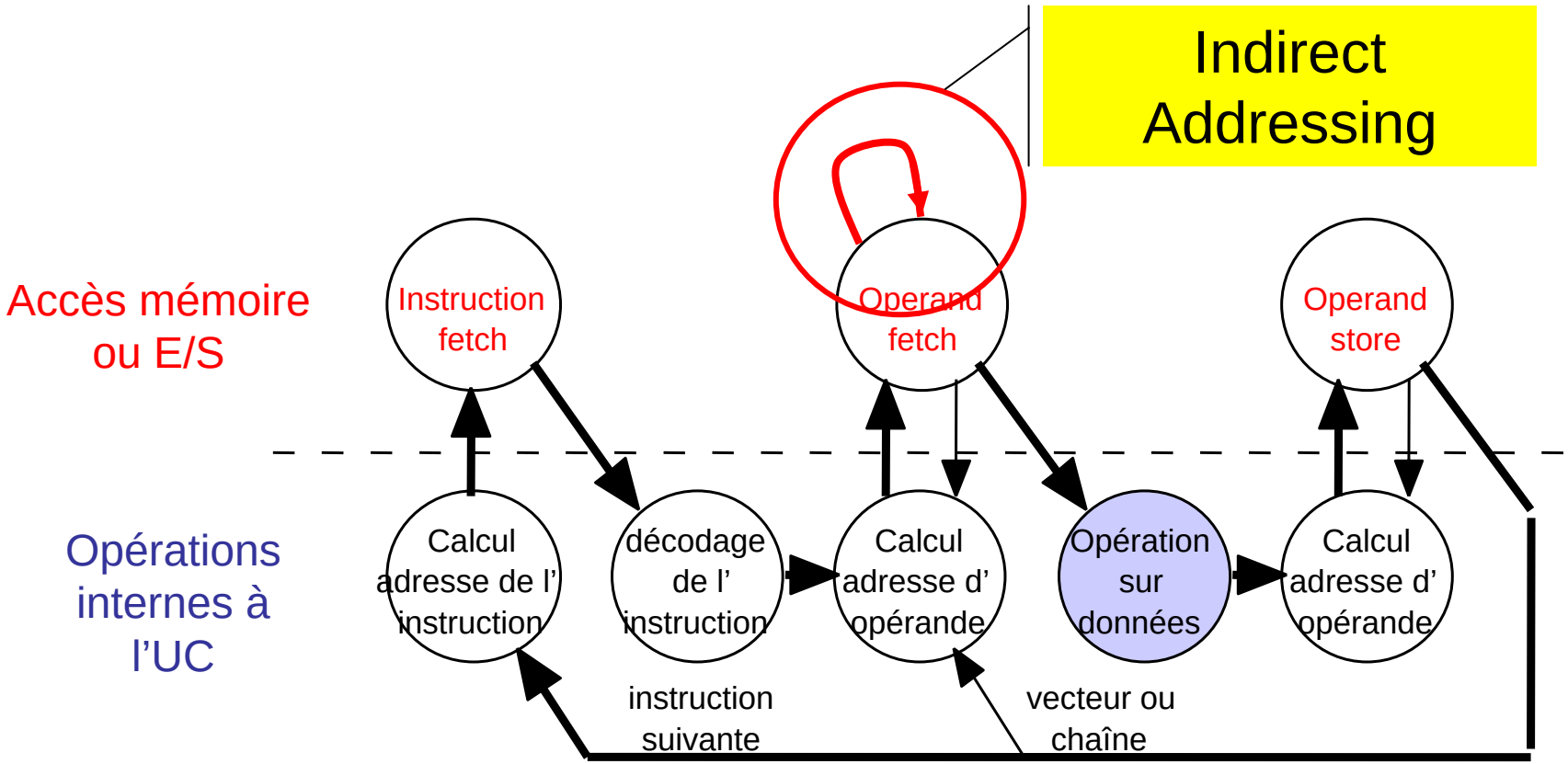


Instruction Fetch

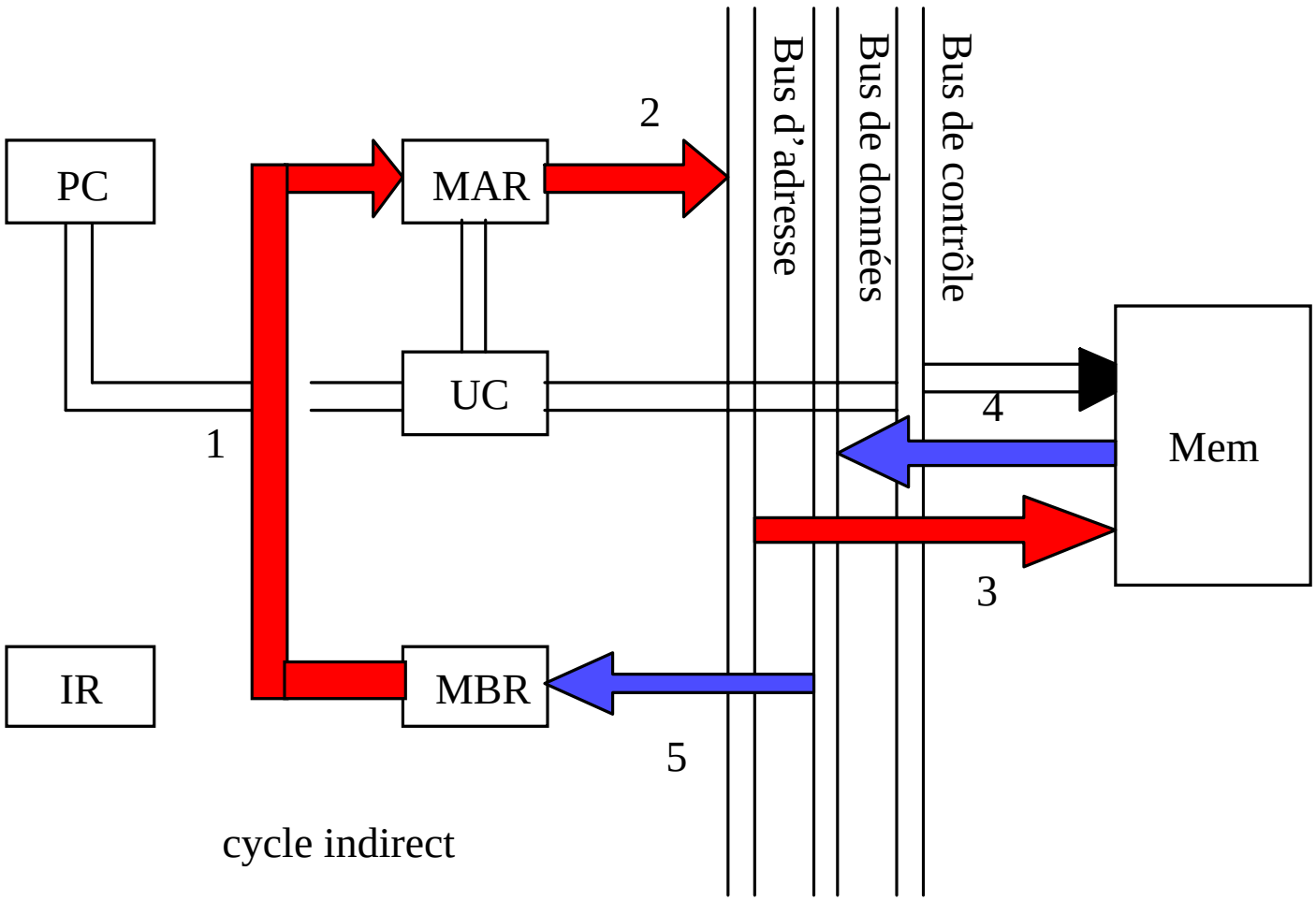


"Fetch" instruction

Instruction Cycle

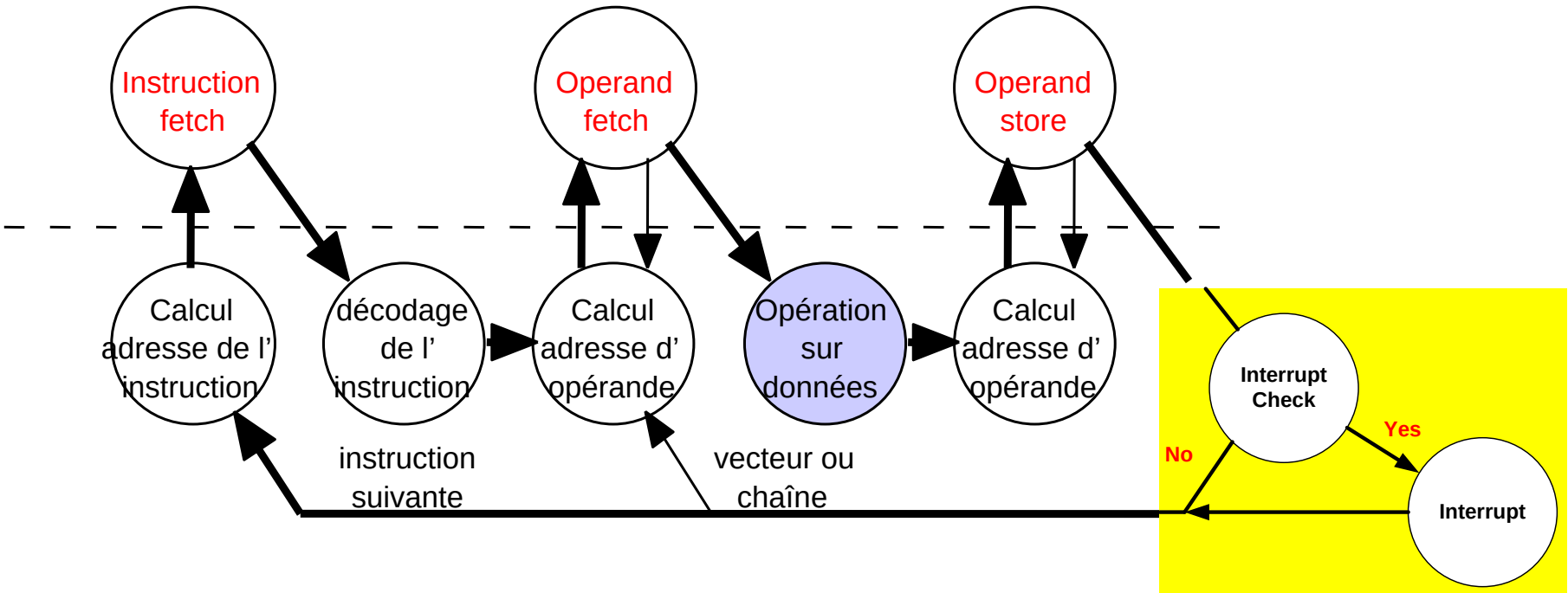


Indirect Cycle

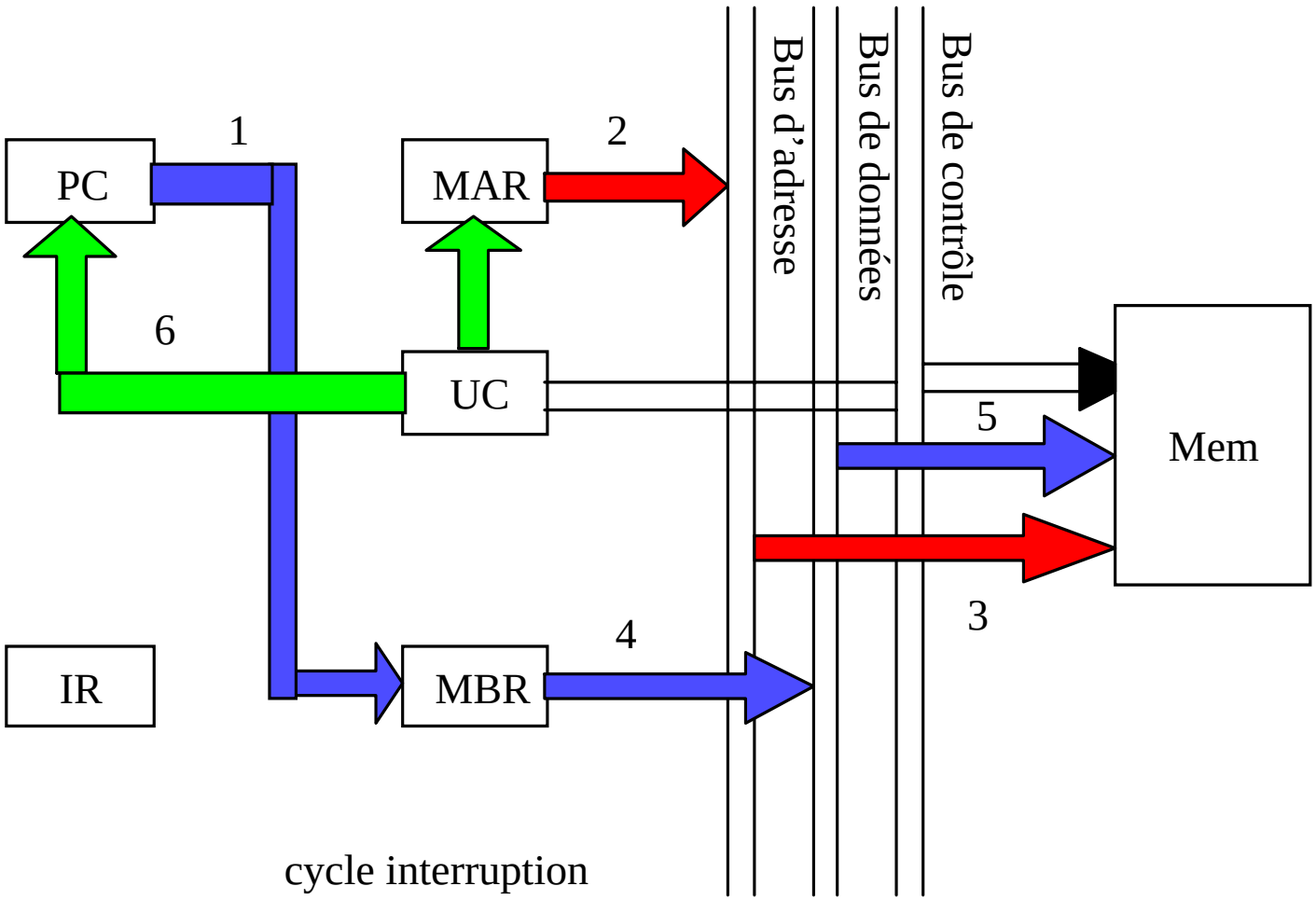


cycle indirect

Instruction Cycle

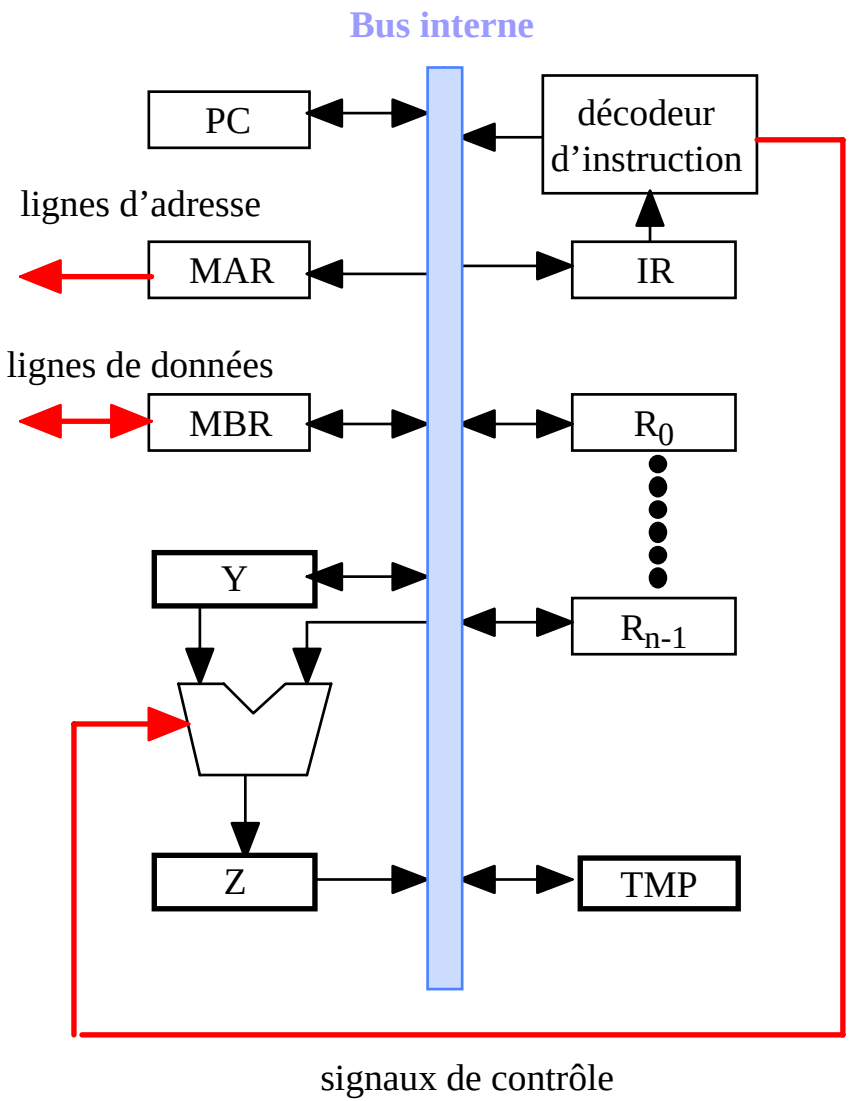


Interruption Cycle

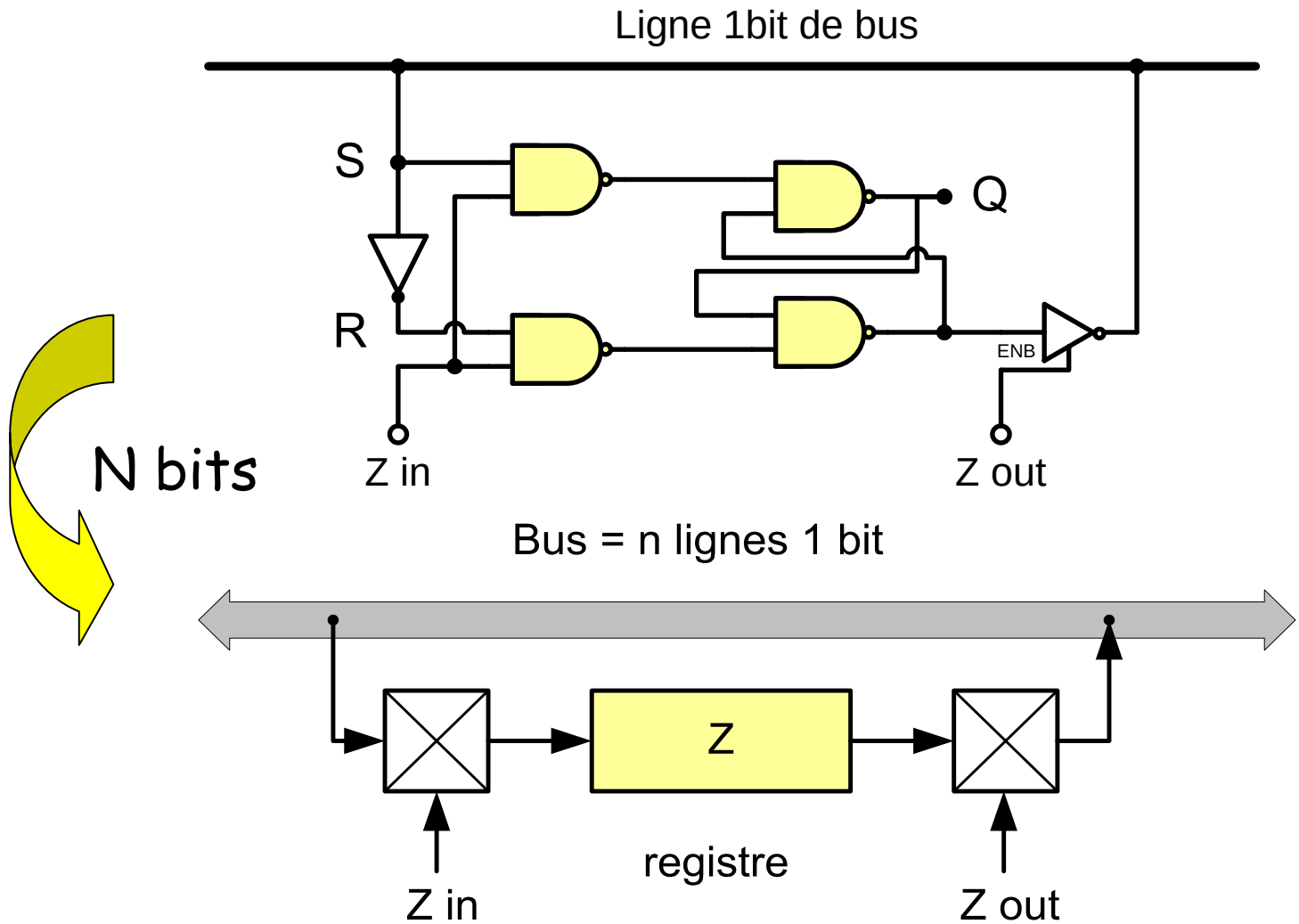


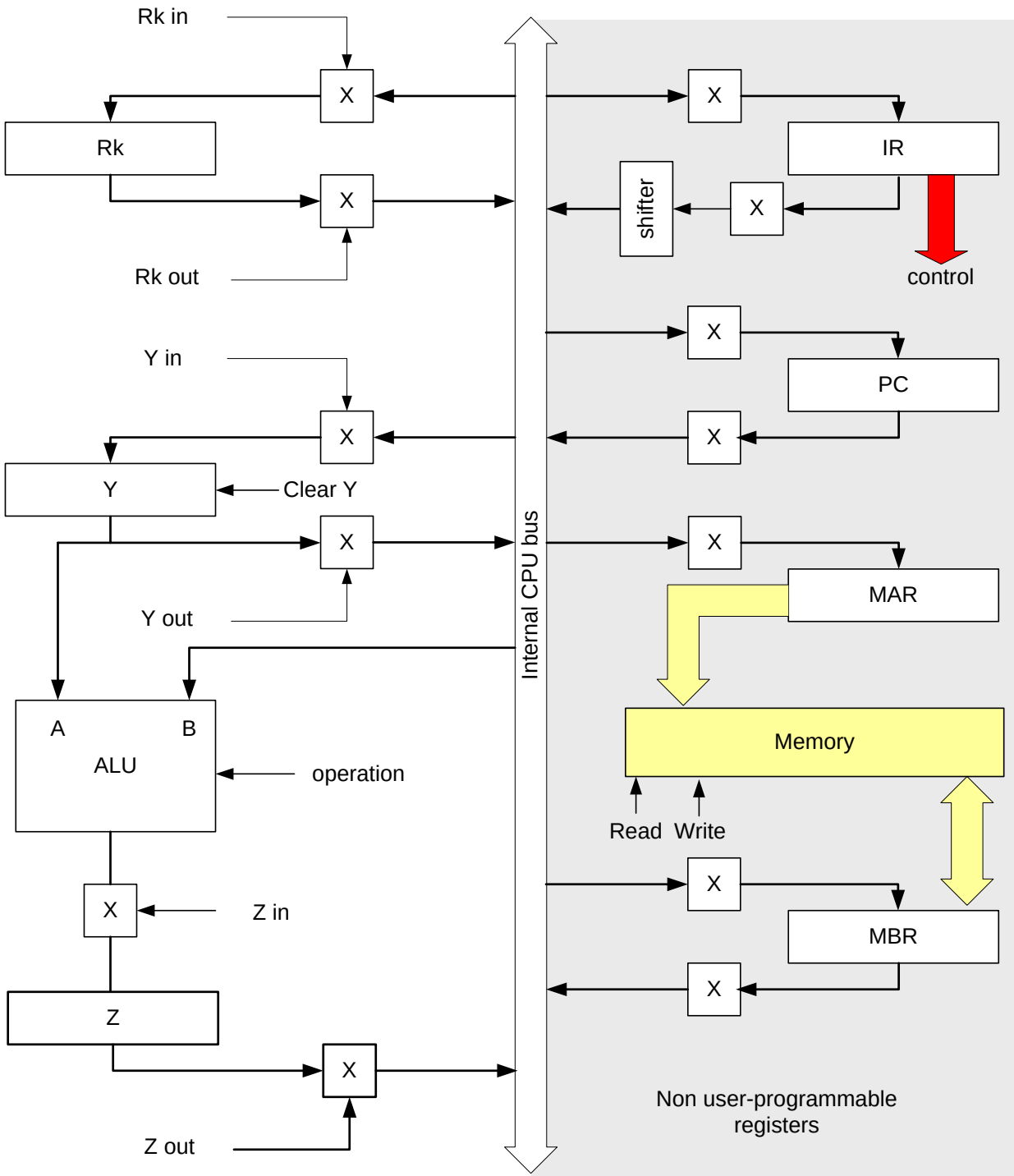
cycle interruption

1-Bus CPU Organization

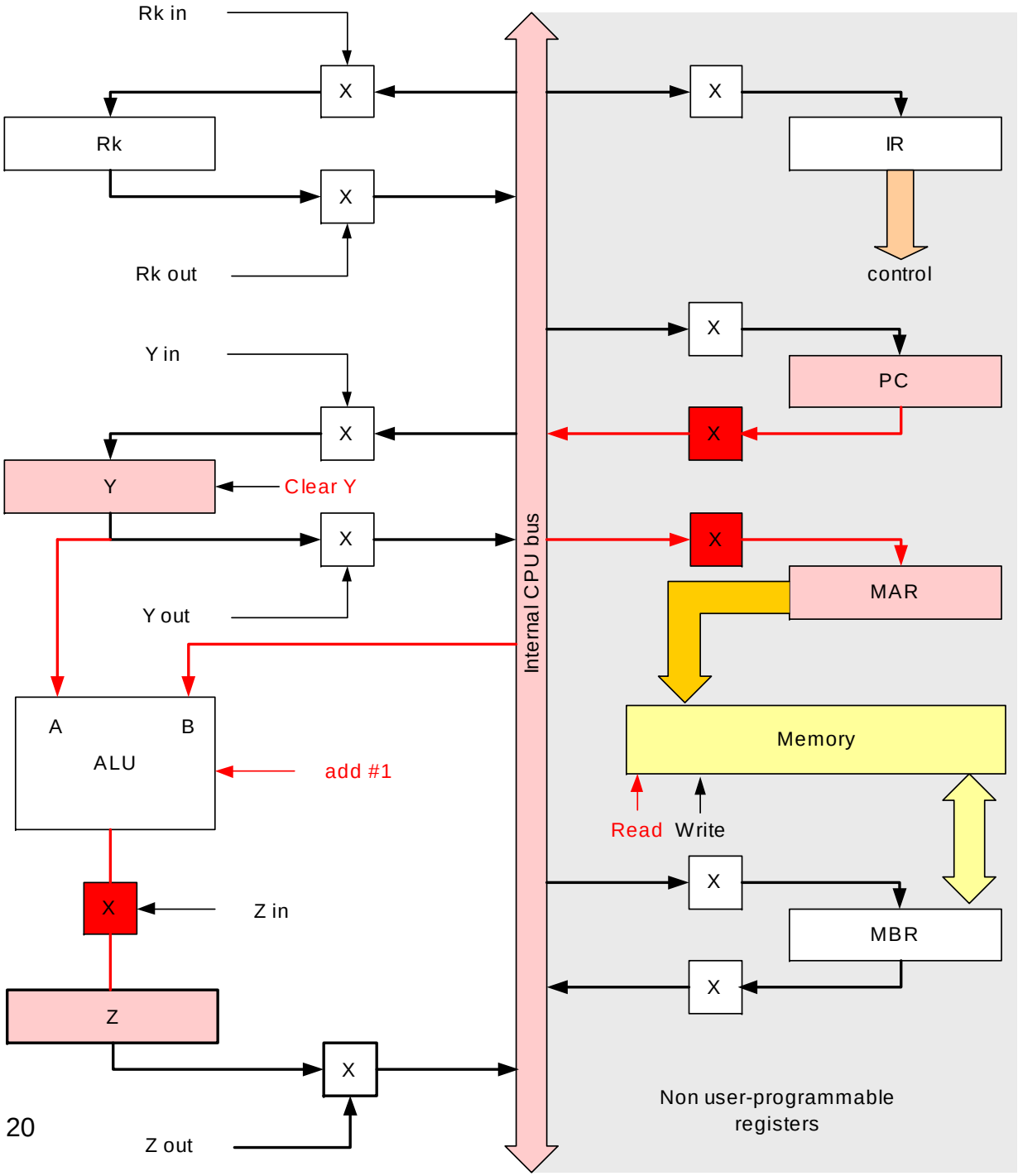


Mémorisation





CPU à un seul bus interne

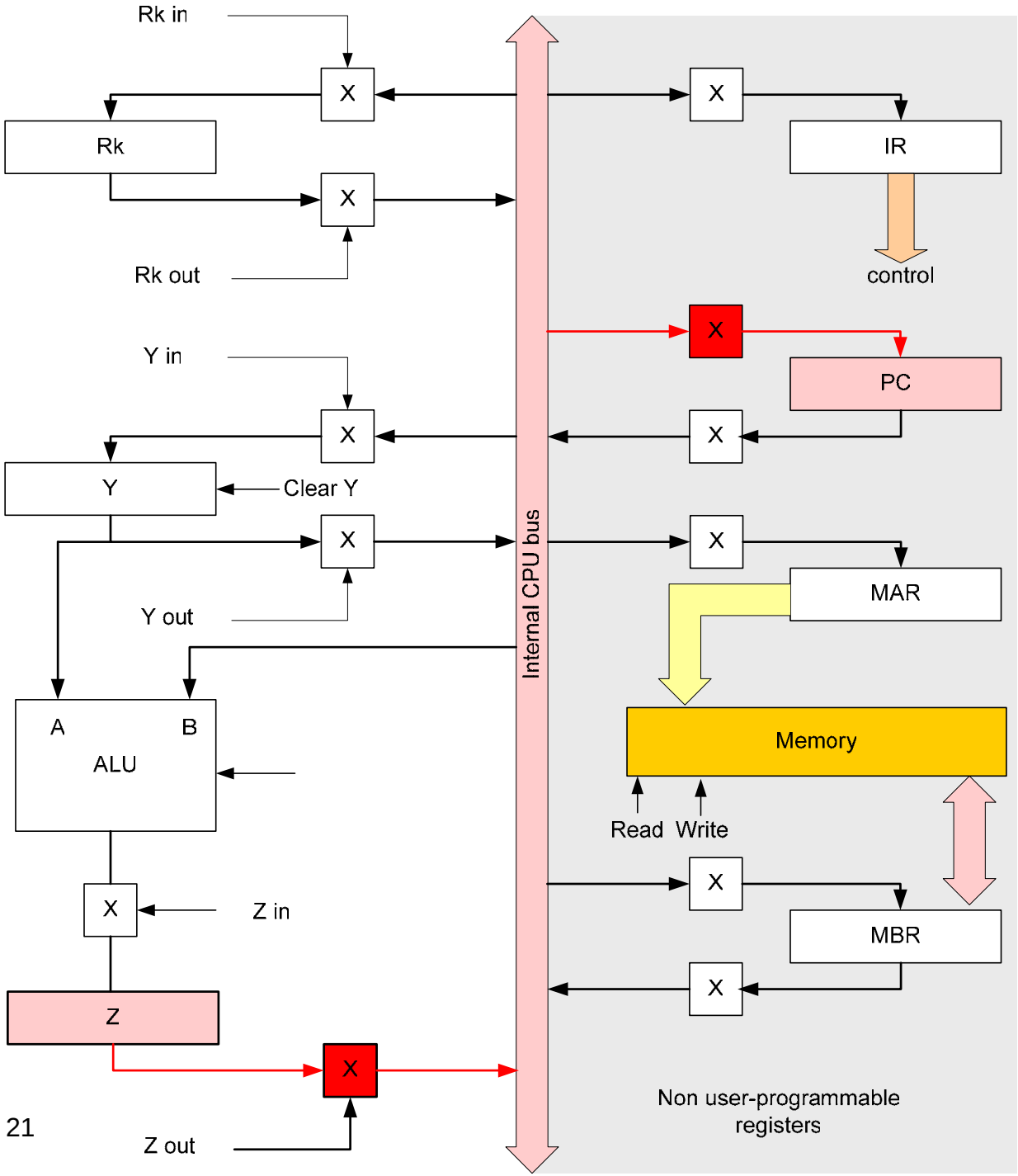


Exemple d'addition

Reg[R1]←
Reg[R1] +
Mem[Reg[R3]]

Phase 1:

- PCout
- MARin
- Read
- Clear Y
- Set CarryIn
- Add
- Zin



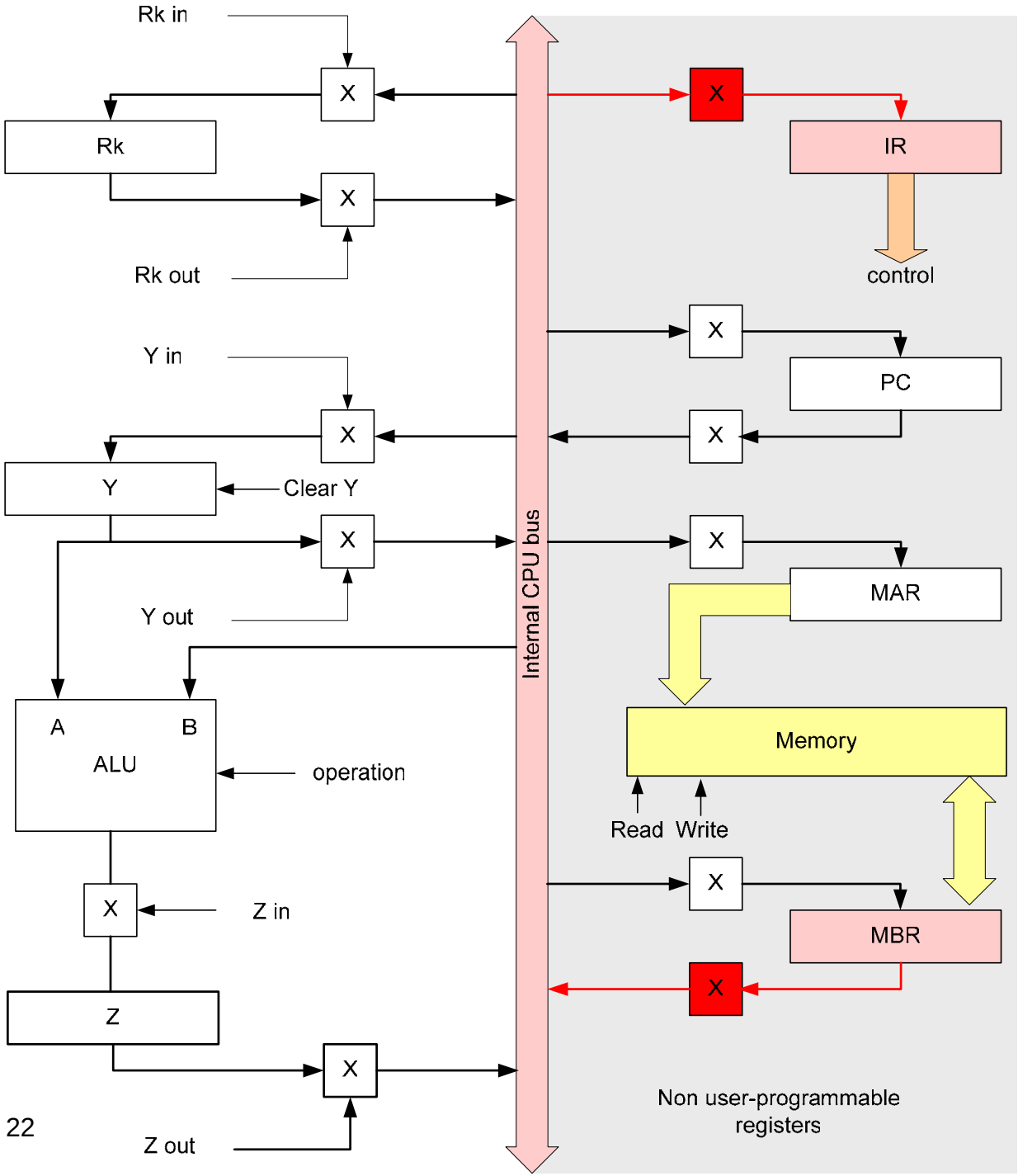
Exemple d'addition

Phase 2:

- Zout
- PCin
- Wait MFC

MFC=

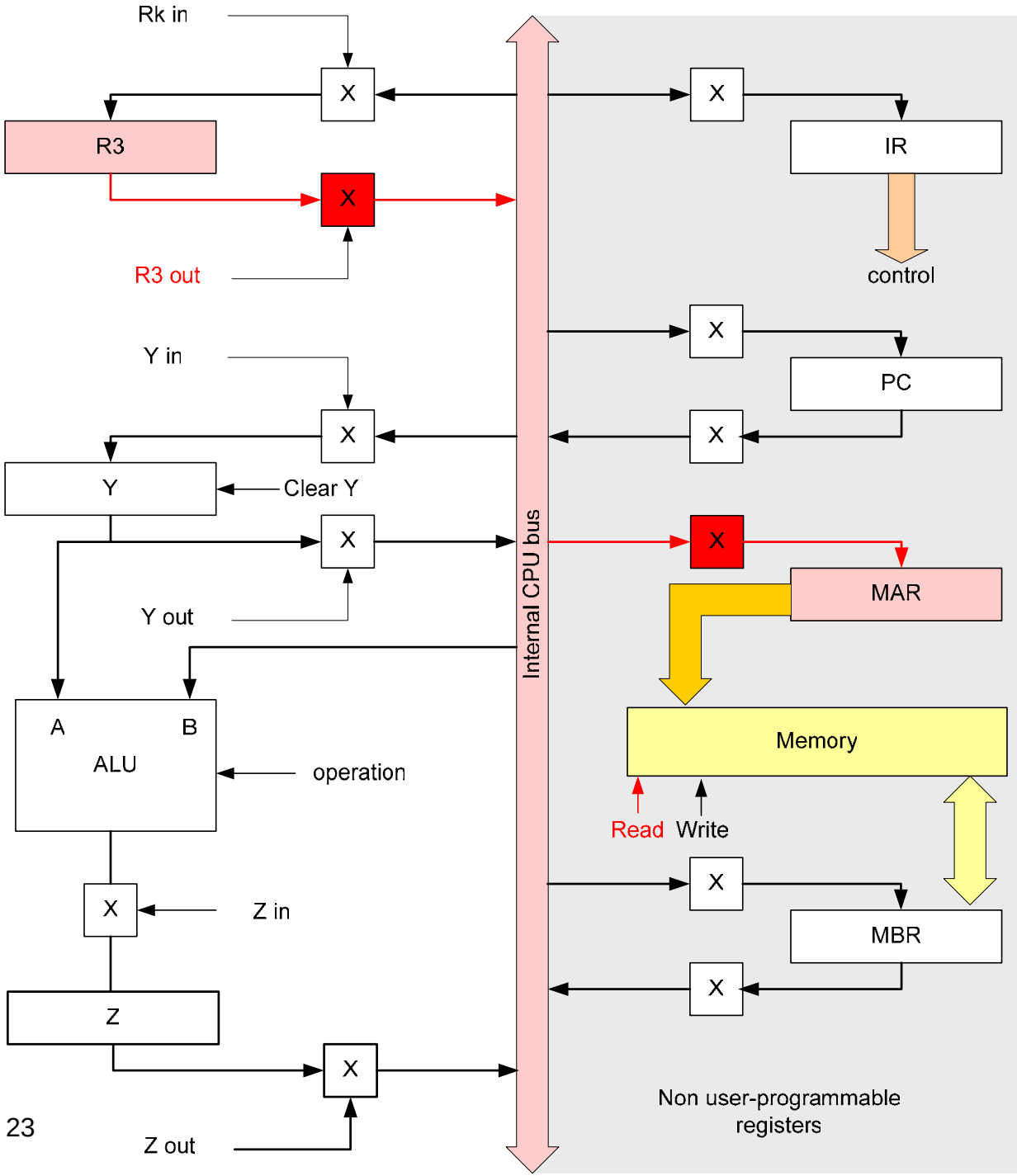
Memory
Function
Completed



Exemple d'addition

Phase 3:

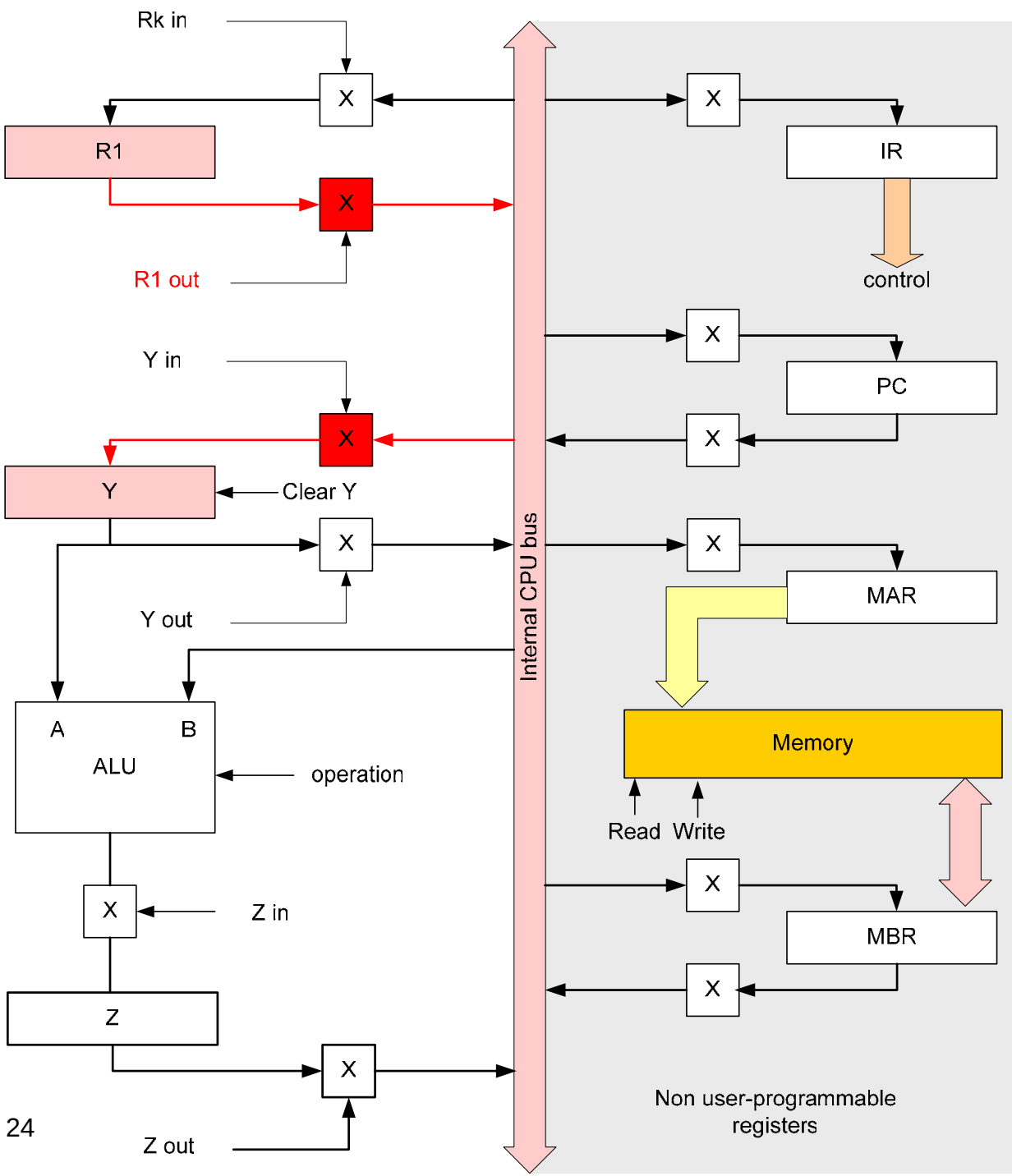
- MBRout
- IRin



Exemple d'addition

Phase 4:

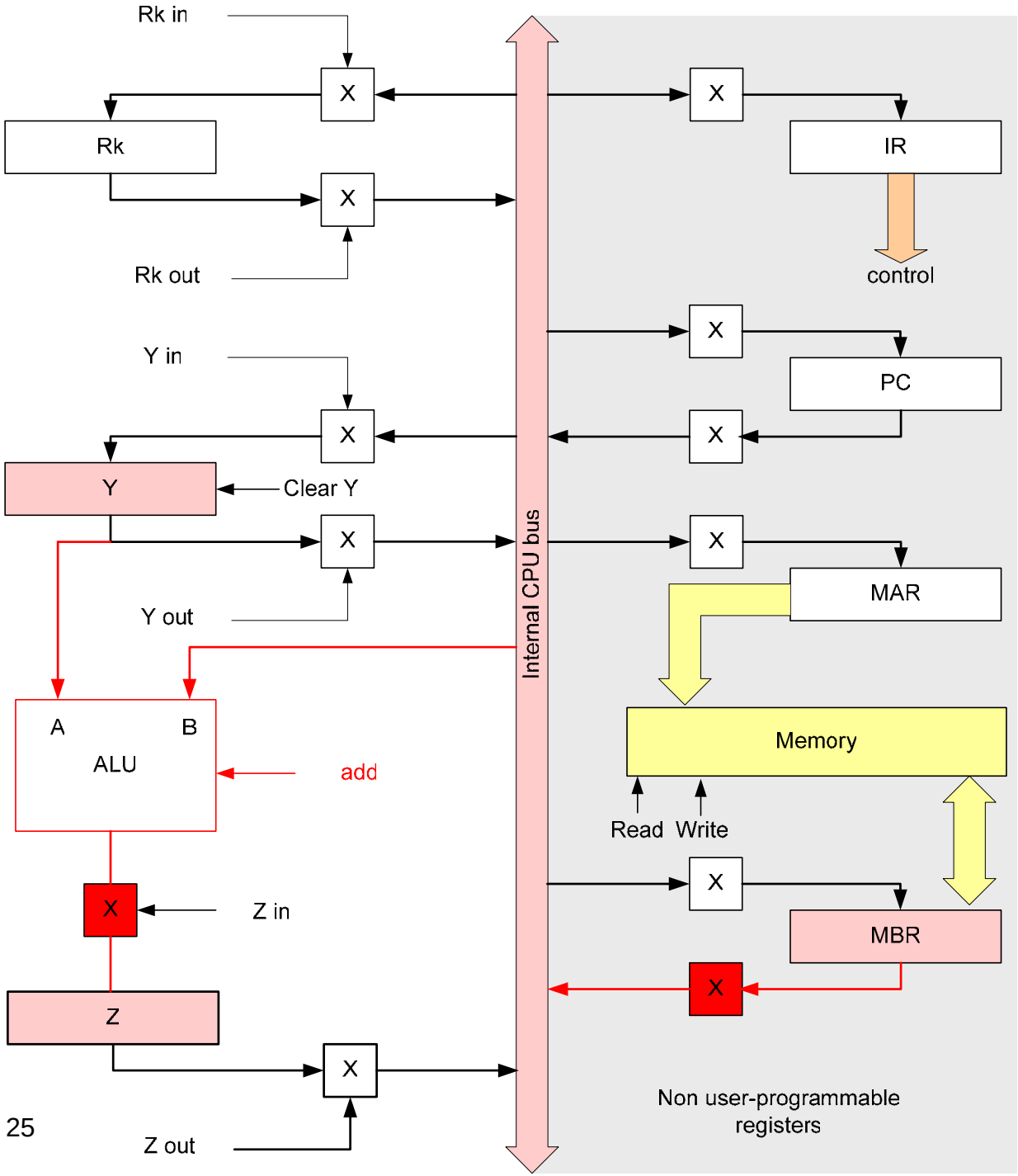
- R3out
- MARin
- Read



Exemple d'addition

Phase 5:

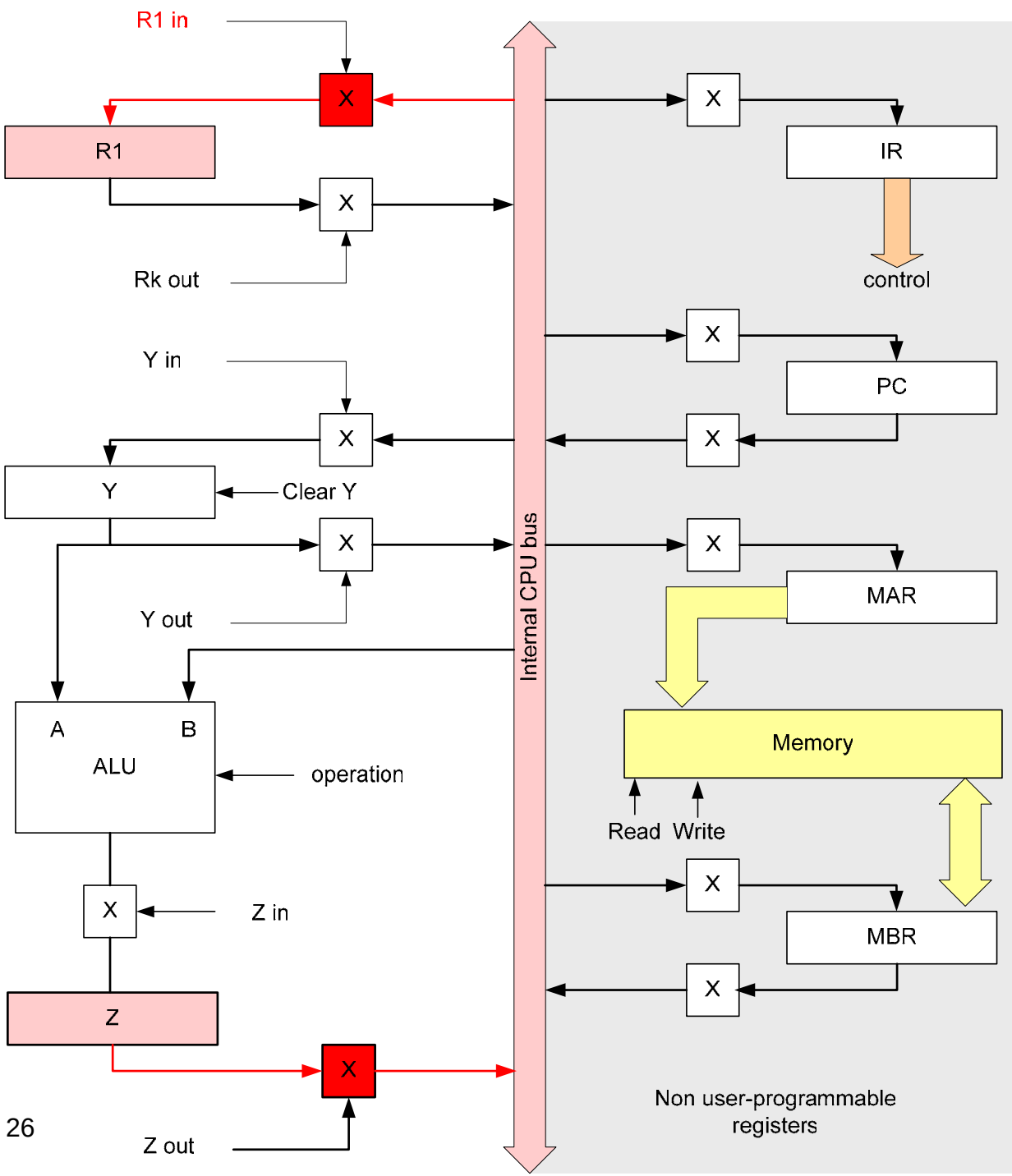
- R1out
- Yin
- Wait MFC



Exemple d'addition

Phase 6:

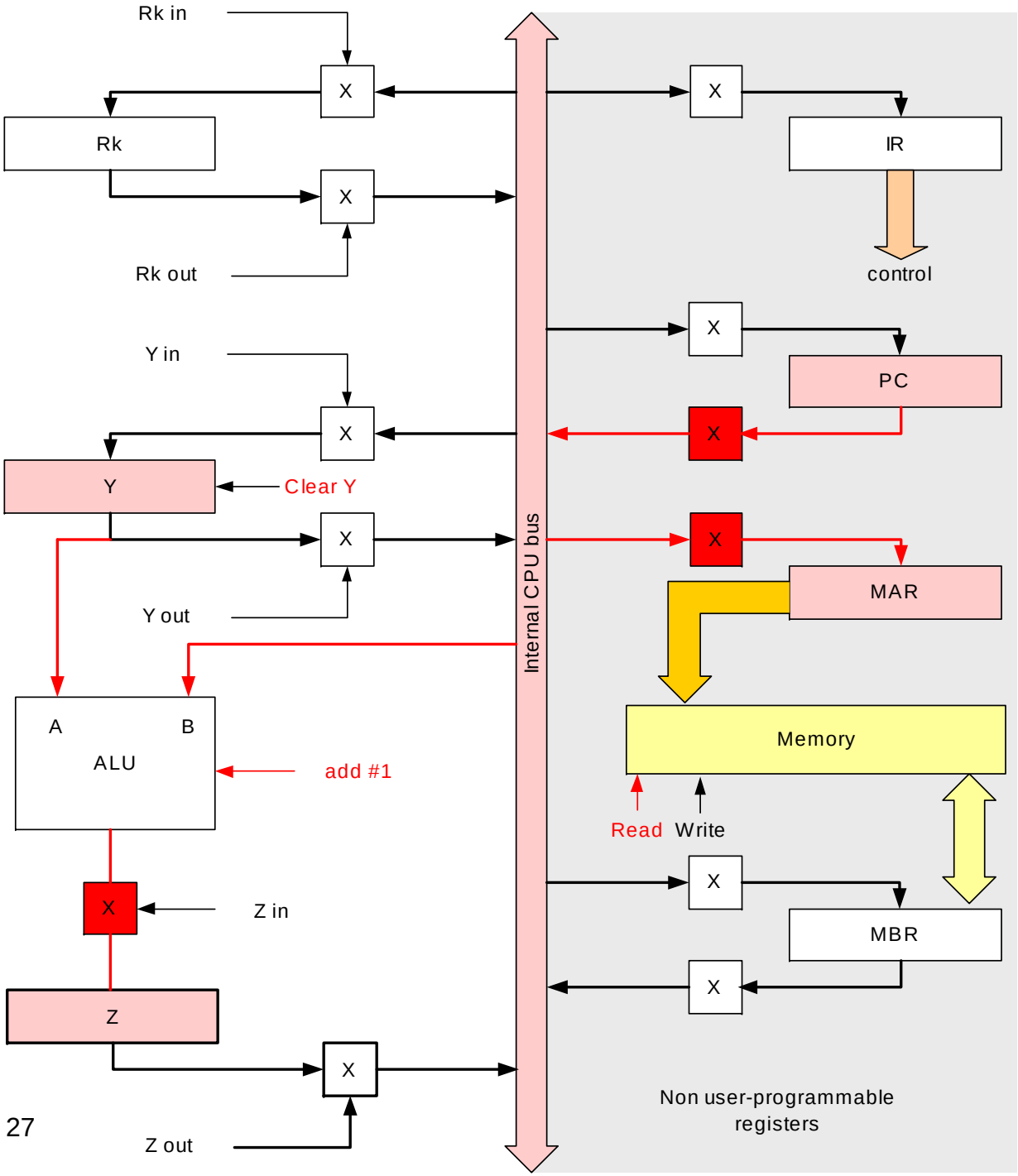
- MBRout
- Zin
- Add



Exemple d'addition

Phase 7:

- Zout
- R1in

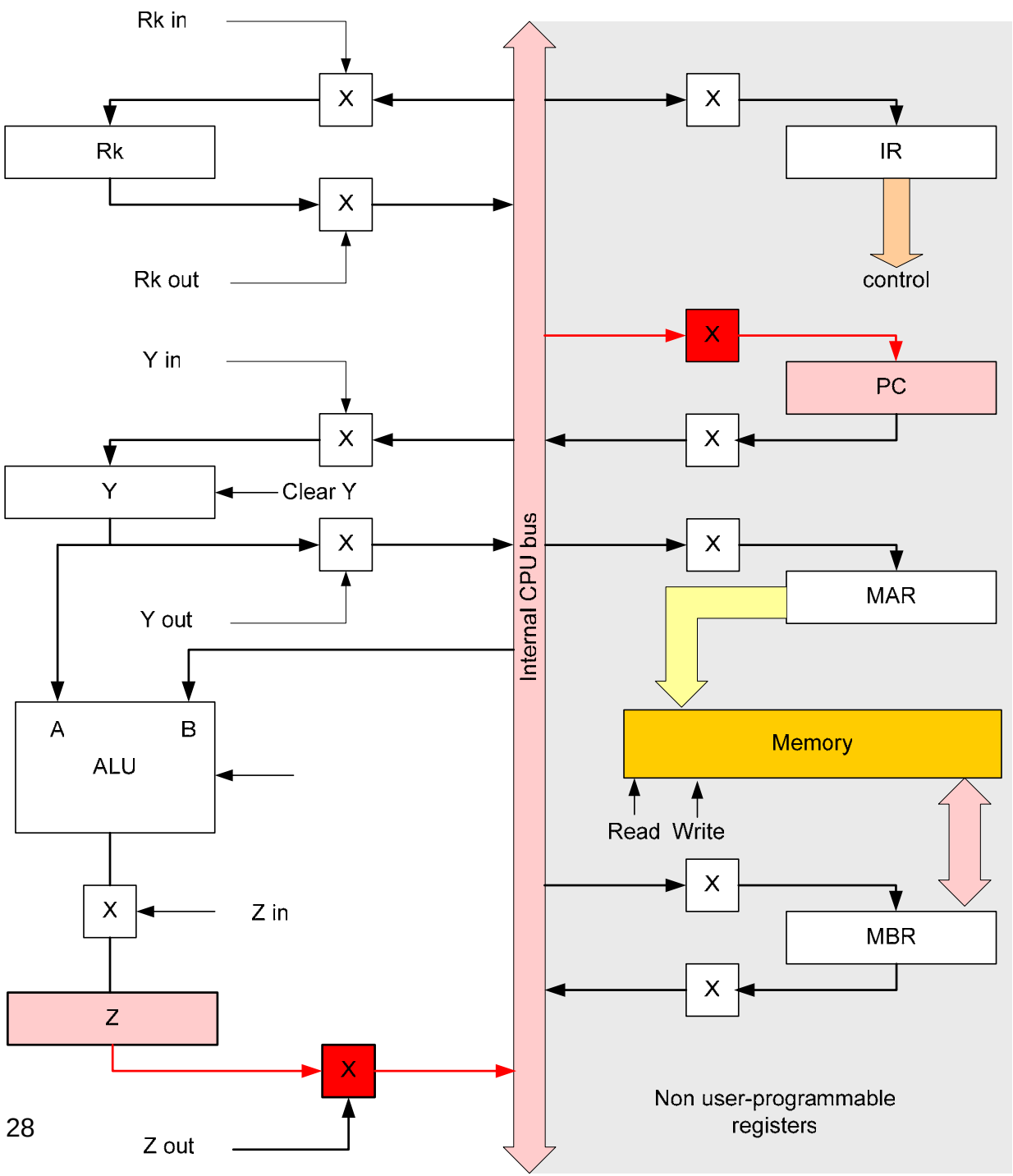


Exemple de branchement

Reg[PC]← Reg[PC]+1+d

Phase 1:

- PCout
- MARin
- Read
- Clear Y
- Set CarryIn
- Add
- Zin



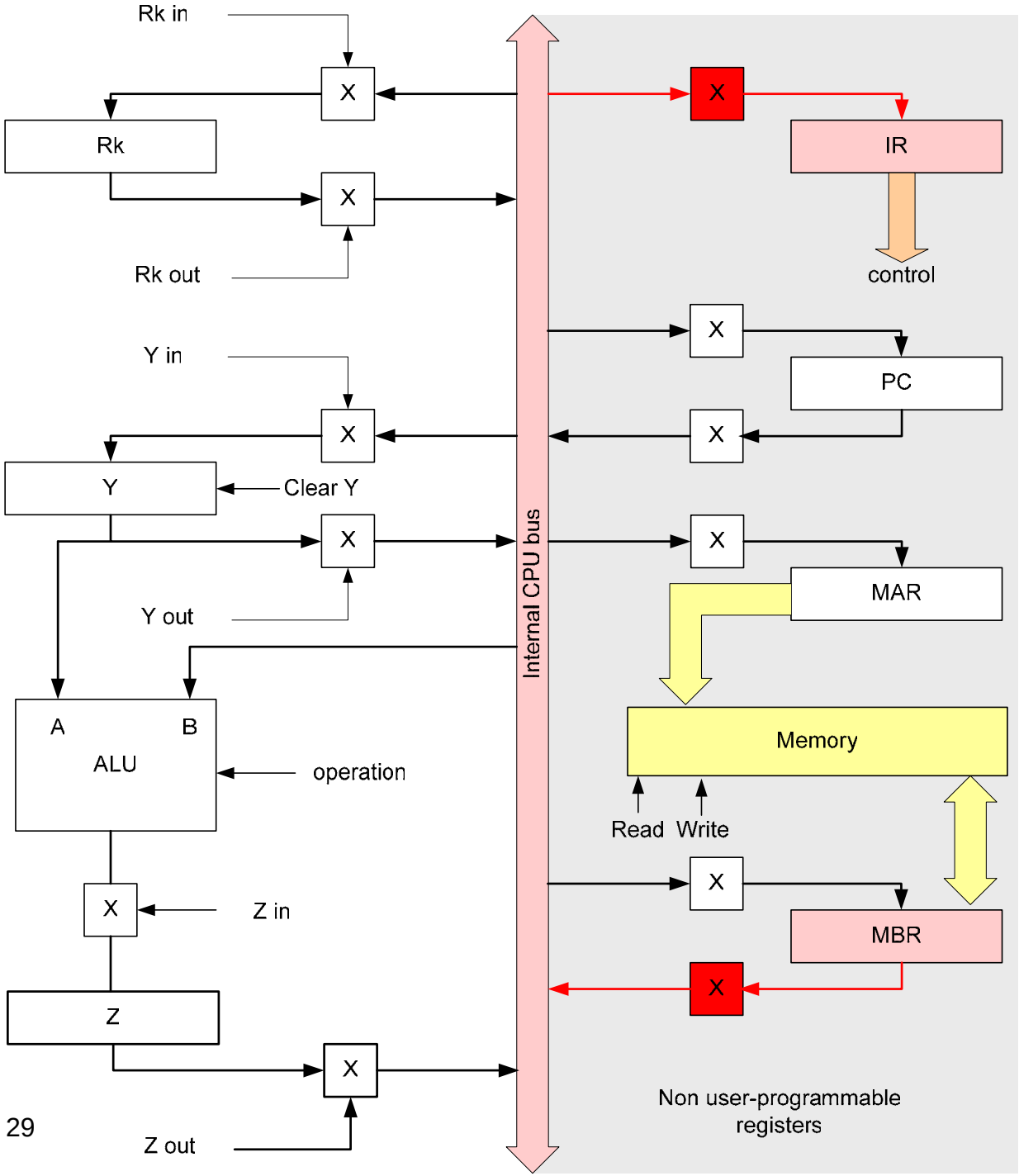
Exemple de branchement

Phase 2:

- Zout
- PCin
- Wait MFC

MFC=

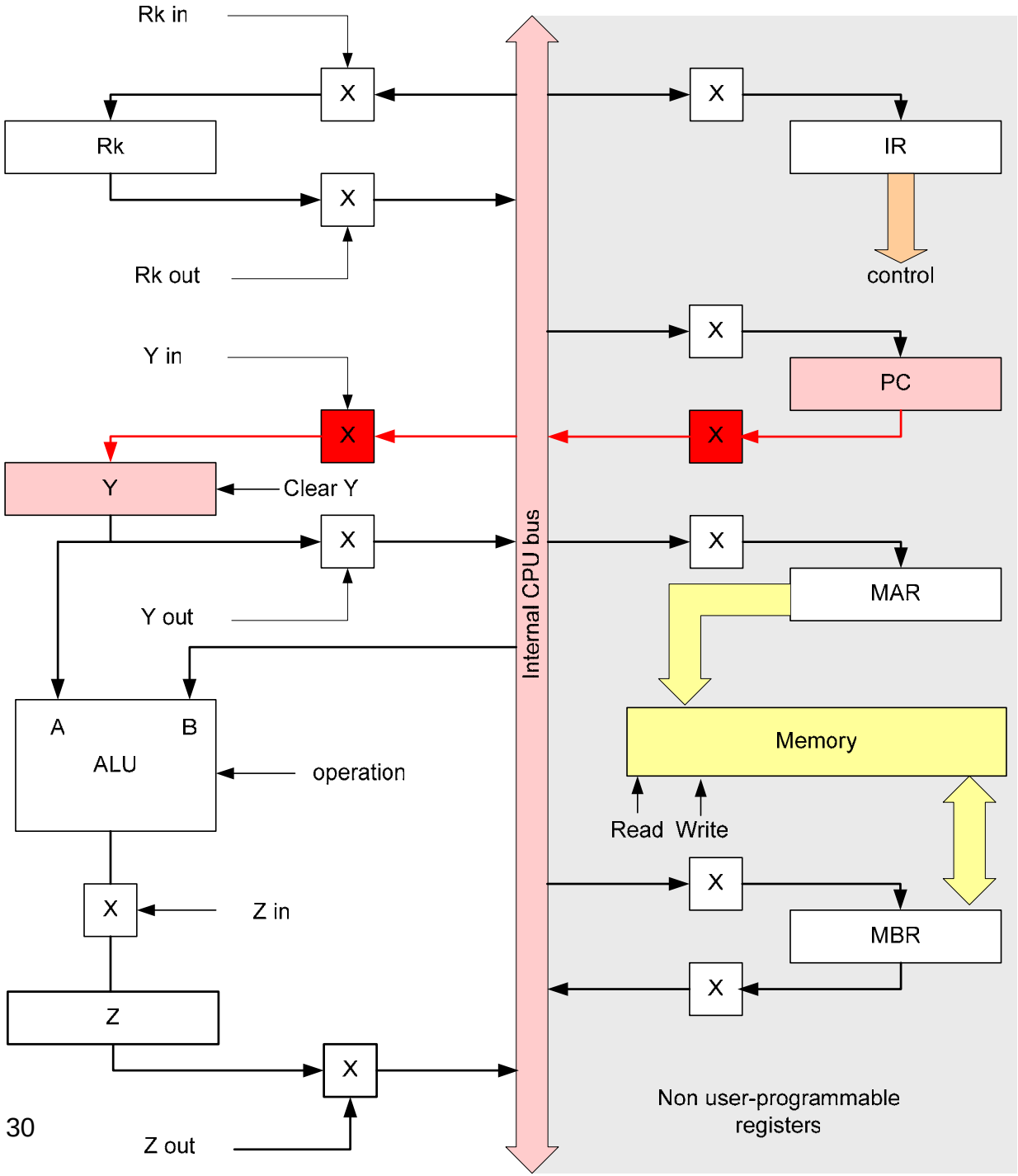
Memory Function Completed



Exemple de branchement

Phase 3:

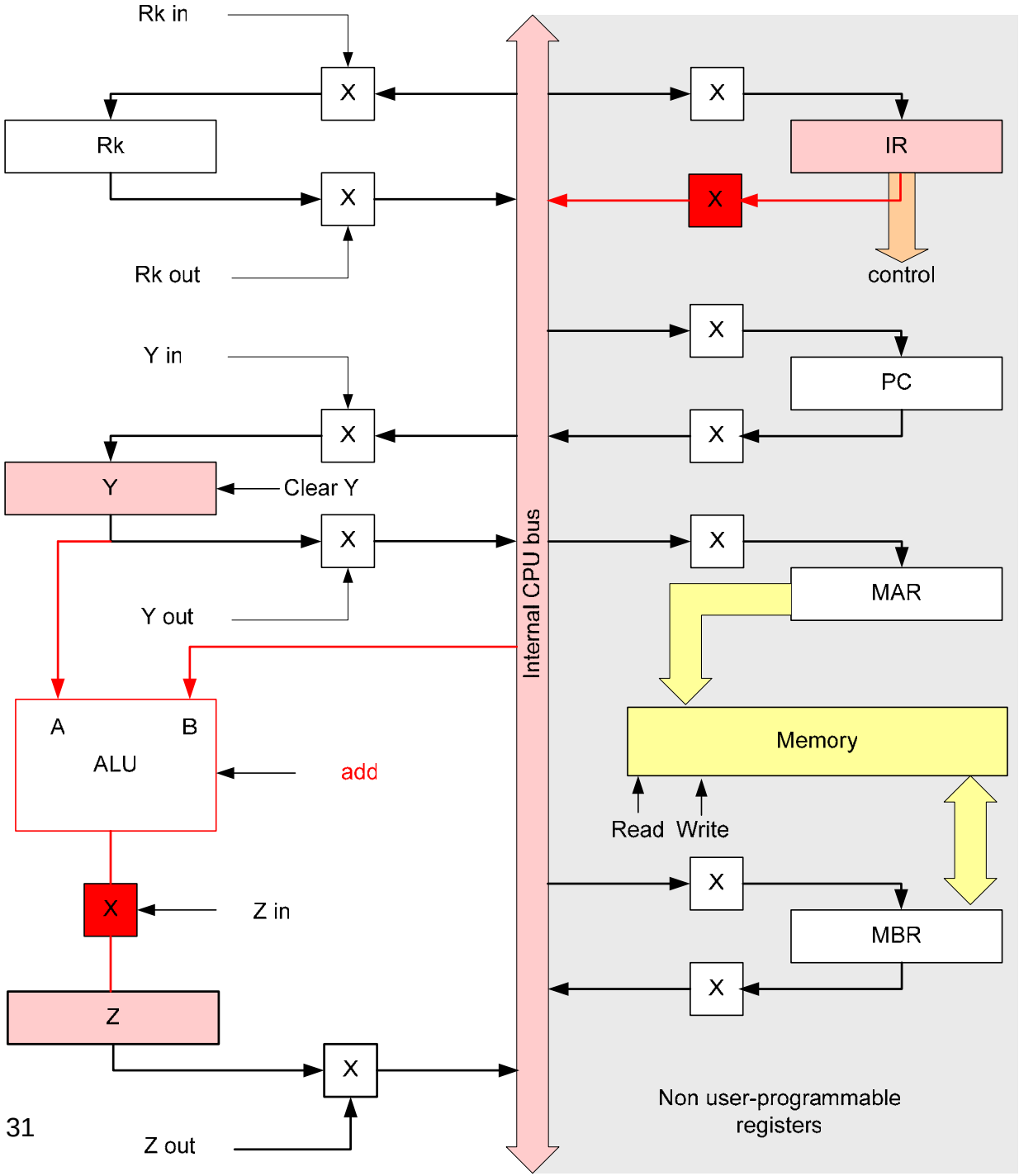
- MBRout
- IRin



Exemple de branchement

Phase 4:

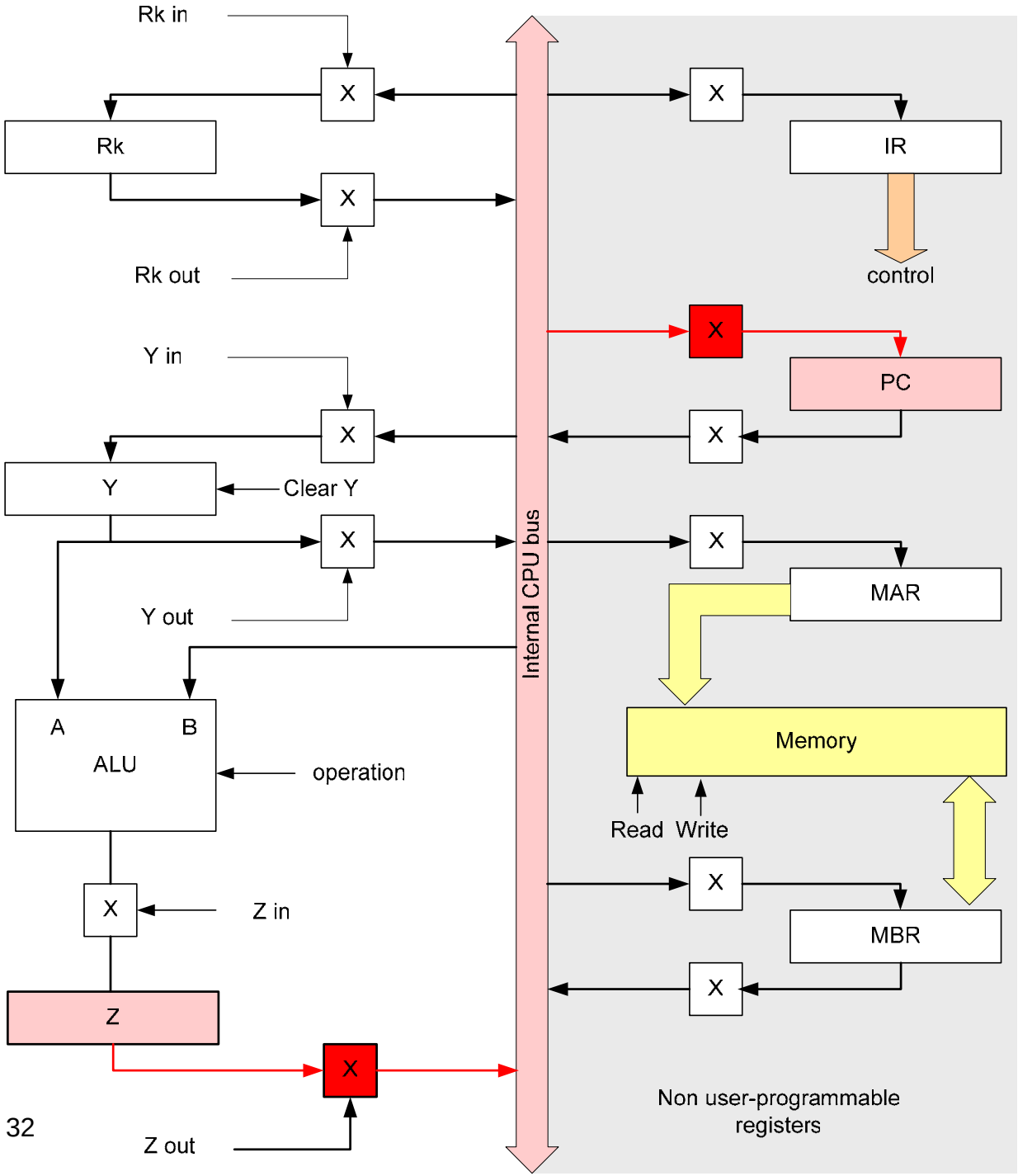
- PCout
- Yin



Exemple de branchement

Phase 5:

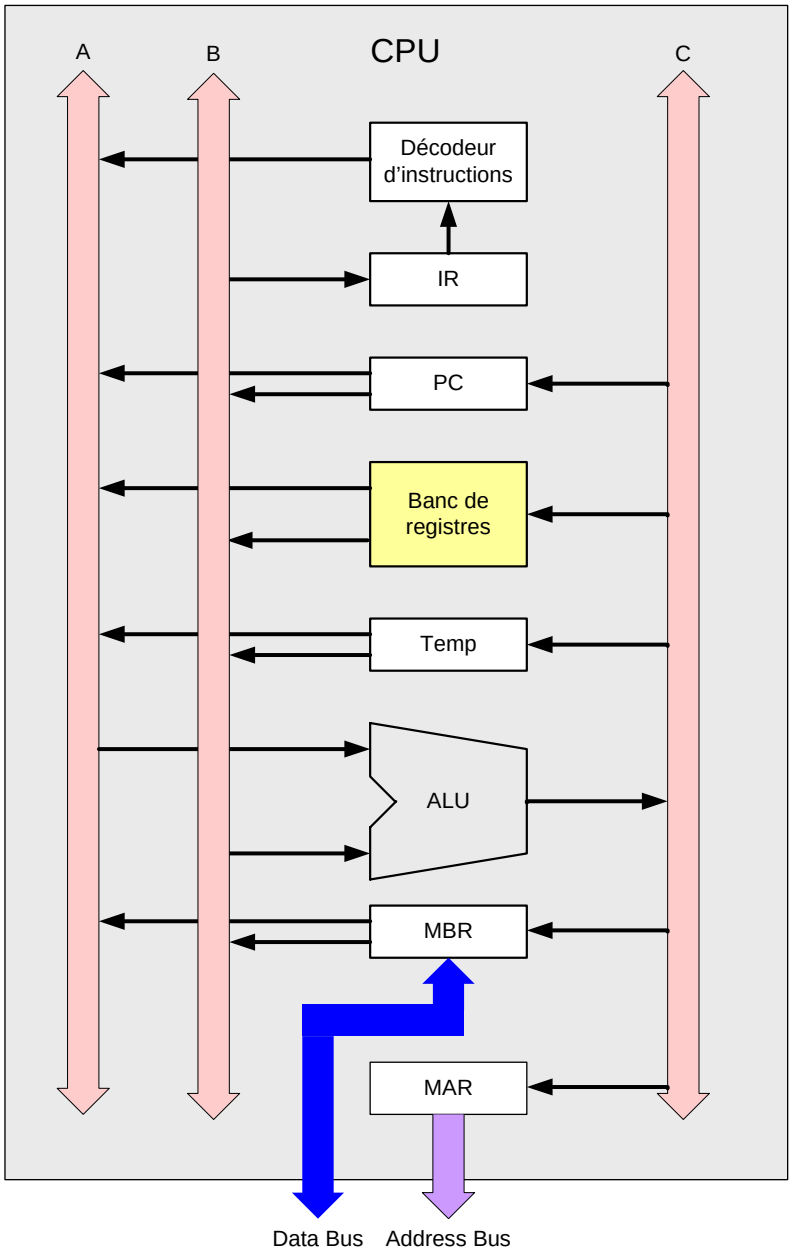
- IRout
- & shift_mask
- Add
- Zin



Exemple de branchement

Phase 6:

- Zout
- PCin



CPU à 3 busses internes

Unité Centrale Complète