Designing a QR Factorization for Multicore and Multi-GPU Architectures using Runtime Systems

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Joint work with University of Tennessee and INRIA Runtime

Vers la simulation numérique pétaflopique sur architectures parallèles hybrides

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University of Colorado Denver | Anschutz Medical Campus

Motivation

Algorithm / Software design

"Must rethink the design of our software."

J. Dongarra, yesterday's talk.

QR factorization

"One algorithmic idea in numerical linear algebra is more important than all the others: QR factorization." L. N. Trefethen and D. Bau, Numerical Linear Algebra, <u>SIAM</u>, 1997.

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High-level algorithm

Runtime System

Device kernels

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QR Factorization Over Runtime Systems

High-level algorithm

Runtime System

Device kernels

CPU core

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QR Factorization Over Runtime Systems

High-level algorithm



High-level algorithm



High-level algorithm



Objective of the talk

Show that this 3-layers programmation paradigm:

- increases productivity;
- * enables performance portability.

Showing everything you have ever wondered about QR factorization.

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- increases productivity;
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© Knowing everything you have ever wondered about QR factorization.

Outline

- 1. QR factorization
- 2. Runtime System for multicore architectures
- 3. Using Accelerators
- 4. Enhancing parallelism
- 5. Distributed Memory

Outline

1. QR factorization

2. Runtime System for multicore architectures

- 3. Using Accelerators
- 4. Enhancing parallelism
- 5. Distributed Memory

High-level algorithm

QR factorization

Device kernels	
CPU core	GPU

Motivation for tile algorithms

Need to design new algorithm in order to

- ★ reduce communication
- ★ enhance parallelism

QR factorization

1D tile QR - binary tree

Reduce Algorithms: Introduction The QR factorization of a long and skinny matrix with its data partitioned

vertically across several processors arises in a wide range of applications.



Reduce Algorithms: Introduction

Example of applications:

- a) in linear least squares problems which the number of equations is extremely larger than the number of unknowns
- b) in block iterative methods (iterative methods with multiple right-hand sides or iterative eigenvalue solvers)
- c) in dense large and more square QR factorization where they are used as the panel factorization step

Reduce Algorithms: Introduction

Example of applications:

- a) in block iterative methods (iterative methods with multiple right-hand sides or iterative eigenvalue solvers),
- b) in dense large and more square QR factorization where they are used as the panel factorization step, or more simply
- c) in linear least squares problems which the number of equations is extremely larger than the number of unknowns.

The main characteristics of those three examples are that

- a) there is only one column of processors involved but several processor rows,
- b) all the data is known from the beginning,
- c) and the matrix is dense.

Various methods already exist to perform the QR factorization of such matrices:

- a) Gram-Schmidt (mgs(row),cgs),
- b) Householder (qr2, qrf),
- c) or CholeskyQR.

We present a new method:

Allreduce Householder (rhh_qr3, rhh_qrf).

The CholeskyQR Algorithm

SYRK:	$C := A^T A$	(mn²)
CHOL:	R := chol(C)	(n³/3)
TRSM:	Q := A/R	(mn²)



Bibligraphy

- A. Stathopoulos and K. Wu, A block orthogonalization procedure with constant synchronization requirements, *SIAM Journal on Scientific Computing*, 23(6):2165-2182, 2002.
- · Popularized by iterative eigensolver libraries:
 - 1) PETSc (Argonne National Lab.) through BLOPEX (A. Knyazev, UCDHSC),
 - 2) HYPRE (Lawrence Livermore National Lab.) through BLOPEX,
 - Trilinos (Sandia National Lab.) through Anasazi (R. Lehoucq, H. Thornquist, U. Hetmaniuk),
 - 4) PRIMME (A. Stathopoulos, Coll. William & Mary).

Parallel distributed CholeskyQR

The CholeskyQR method in the parallel distributed context can be described as follows:

1: SYRK:	C:= A ^T A	(mn²)	1.	$\overline{C_i} \leftarrow \overline{A_i^T}_{A_i}$
2: MPI_Reduce: 3: CHOL:	C:= sum _{procs} C R := chol(C)	(on proc 0) (n³/3)	2. 3-4	$\begin{array}{c} \\ \\ \leftarrow\\ \\ c_1 \\ +\\ \\ c_2 \\ +\\ \\ c_3 \\ +\\ \\ c_4 \\ \end{array}$
4: MPI_Bdcast	Broadcast the R fa	actor on proc 0 ocessors	5.	
5: TRSM:	Q := A/R	(mn²)		Q _i A _i

In this experiment, we fix the problem: m=100,000 and n=50.

Efficient enough?





(... and, OK, you might want to add an MPI user defined datatype to send only the upper part of R)



Parallel distributed CholeskyQR

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2: MPI_Reduce:	C:= sum _{procs} C	(on proc 0)	
3: CHOL:	R := chol(C)	(n³/3)	
4: MPI_Bdcast	Broadcast the R factor on proc 0		
	to all the other processors		
5: TRSM:	Q := A/R	(mn²)	



This method is extremely fast. For two reasons:

1. first, there is only one or two communications phase,

2. second, the local computations are performed with fast operations.

Another advantage of this method is that the resulting code is exactly four lines,

so the method is simple and relies heavily on other libraries.

Despite all those advantages,

4. this method is highly unstable.





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On two processes

time




















Latency but also possibility of fast

panel factorization.

- DGEQR3 is the recursive algorithm (see Elmroth and Gustavson, 2000), DGEQRF and DGEQR2 are the LAPACK routines.
- Times include QR and DLARFT.
- Run on Pentium III.







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When only R is wanted: The MPI_Allreduce

In the case where only R is wanted, instead of constructing our own tree, one can simply use MPI_Allreduce with a user defined operation. The operation we give to MPI is basically the Algorithm 2. It performs the operation:



This **binary** operation is **associative** and this is all MPI needs to use a user-defined operation on a user-defined datatype. Moreover, if we change the signs of the elements of R so that the diagonal of R holds positive elements then the binary operation **Rfactor** becomes **commutative**.

The code becomes two lines:

lapack_dgeqrf(mloc, n, A, lda, tau, &dlwork, lwork, &info); MPI_Allreduce(MPI_IN_PLACE, A, 1, MPI_UPPER, LILA_MPIOP_QR_UPPER, mpi_comm);



QR factorization



Grid 5000



Latency (ms)	Orsay	Toulouse	Bordeaux	Sophia
Orsay	0.07	7.97	6.98	6.12
Toulouse		0.03	9.03	8.18
Bordeaux			0.05	7.18
Sophia				0.06
Throughput (Mb/s)	Orsay	Toulouse	Bordeaux	Sophia
~				
Orsay	890	78	90	102
Orsay Toulouse	890	78 890	90 77	102 90
Orsay Toulouse Bordeaux	890	78 890	90 77 890	102 90 83



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QR Factorization Over Runtime Systems





Consider **architecture:** parallel case: *P* processing units **problem:** QR factorization of a *m*-by-*n* TS matrix (TS = $m/P \ge n$) (main) assumption: one processor has at least mn/P part of the matrix and one processor performs at least $\frac{2mn^2}{p}$ flops

\Rightarrow 1D tile QR algorithm with a binary tree

theory:

-	TSQR	ScaLAPACK-like	Lower bound
# flops	$\frac{2mn^2}{P} + \frac{2n^3}{3}\log P$	$\frac{2mn^2}{P} - \frac{2n^3}{3P}$	$\Theta\left(\frac{mn^2}{P}\right)$
# words	$\frac{n^2}{2}\log P$	$\frac{n^2}{2}\log P$	$\frac{n^2}{2}\log P$
# messages	log P	2n log P	log P

Communication for tile algorithms

- ★ tall and skinny matrix, parallel distributed case
 ⇒ 1D tile QR algorithm with a flat tree
- tall and skinny matrix, sequential case
- * general matrix, sequential case
- * general matrix, parallel distributed case

















Consider

architecture: sequential case: one processing unit with cache of size (*W*) **problem:** QR factorization of a *m*-by-*n* TS matrix (TS = $m \ge n$ and $W \ge \frac{3}{2}n^2$)

\Rightarrow 1D tile QR algorithm with a flat tree

theory:

-	flat tree	LAPACK-like	Lower bound
# flops	$2mn^2$	$2mn^2$	$\Theta(mn^2)$
# words	mn	$\frac{m^2n^2}{2W}$	mn
# messages	$\frac{mn}{W}$	$\frac{mn^2}{2W}$	$\frac{mn}{W}$

Communication for tile algorithms

★ tall and skinny matrix, parallel distributed case

\Rightarrow 1D tile QR algorithm with a flat tree

* tall and skinny matrix, sequential case

\Rightarrow 1D tile QR algorithm with a flat tree

- * general matrix, sequential case
- * general matrix, parallel distributed case

2D tile QR



2D tile QR







1. dgeqrt(A[0][0], T[0][0]);





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dgeqrt(A[0][0], T[0][0]);
 dlarfb(A[0][0], T[0][0], A[0][1]);





1. dgeqrt(A[0][0], T[0][0]); 2. dlarfb(A[0][0], T[0][0], A[0][1]);




















 $\label{eq:constraints} \begin{array}{l} \mbox{for} (k=0); k<TLES; k+1 \} \{ & \mbox{degret}(k|k|, Tk[|k|], k|k|](n); \\ \mbox{for} (n=k+1; n<TLES; n++) \{ & \mbox{degret}(k|k|, A|k|||k|, A|k|](n); \\ \mbox{for} (n=k+1; n<TLES; n++) \{ & \mbox{degret}(k|k|, A|m||k|, A|k|](n); \\ \mbox{for} (n=k+1; n<TLES; n++) \\ & \mbox{degret}(k|k|, A|m||k|, A|k|](n), A|k|[n], A|m|](n); \\ \mbox{for} (n=k+1; n<TLES; n++) \\ \mbox{degret}(k|k|, T|m||k|, A|k|[n], A|k|[n], A|m|](n); \\ \mbox{for} (n=k+1; n<TLES; n++) \\ \mbox{degret}(k|k|, T|m||k|, A|k|[n], A|m|](n); \\ \mbox{for} (n=k+1; n<TLES; n++) \\ \mbox{degret}(k|k|, T|m|](k), A|k|[n], A|m|](n); \\ \mbox{for} (n=k+1; n<TLES; n++) \\ \mbox{degret}(k|m|](k), T|m|](k), A|k|[n], A|m|](n); \\ \mbox{for} (n=k+1; n<TLES; n++) \\ \mbox{for} (n=k+1; n) \\ \mbox{for} (n=k+1$













for (I = 0; k < TLES; k++) {
 digetT(k[k], T[k][k]);
 for (n = k+1; n < TLES; n++) {
 district[k][k], T[k][k], A[k][n]);
 for (m = k+1; n < TLES; m++]
 dtsart(k][k], T[m][k], T[m][k]);
 for (n = k+1; n < TLES; n++)
 dsarb(A[m][k], T[m][k], A[k][n], A[m][n]);
 }
 }
 }
}</pre>

Lower bounds

- 1. Extends previous lower bounds on the volume of communication for matrix-matrix multiplication from
 - Hong and Kung (81) sequential case: $\Omega(\frac{n^3}{\sqrt{M}})$
 - ▶ Irony,Toledo,Tiskin (04) parallel case: $\Omega(\frac{n^2}{\sqrt{P}})$

2. For LU, observe that:

$$\begin{pmatrix} I & 0 & -B \\ A & I & 0 \\ 0 & 0 & I \end{pmatrix} = \begin{pmatrix} I & & \\ A & I & \\ 0 & 0 & I \end{pmatrix} \begin{pmatrix} I & 0 & -B \\ & I & A \cdot B \\ & & I \end{pmatrix}$$

therefore lower bound for matrix-matrix multiply (latency, bandwidth and operations) also holds for LU.

Lower bounds

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- 2. For LU, observe that:

$$\left(\begin{array}{ccc}I&0&-B\\A&I&0\\0&0&I\end{array}\right)=\left(\begin{array}{ccc}I&\\A&I\\0&0&I\end{array}\right)\left(\begin{array}{ccc}I&0&-B\\&I&A\cdot B\\&&I\end{array}\right)$$

therefore lower bound for matrix-matrix multiply (latency, bandwidth and operations) also holds for LU.

2D tile QR - binary tree

	2D tile QR binary tree		ScaLAPACK Algorith	m	Lower bound
# flops	$\left(\frac{4}{3}\right)\cdot\left(n^3/P\right)$	~	$\left(\frac{4}{3}\right)\cdot\left(n^3/P\right)$	✓	$\mathcal{O}\left(n^{3}/P\right)$
# words	$\left(\frac{3}{4} \cdot \log P\right) \cdot \left(n^2/\sqrt{P}\right)$	✓	$\left(\frac{3}{4} \cdot \log P\right) \cdot \left(n^2/\sqrt{P}\right)$	✓	$\mathcal{O}\left(n^2/\sqrt{P}\right)$
# messages	$\left(\frac{3}{8} \cdot \log^3 P\right) \cdot \left(\sqrt{P}\right)$	✓	$\left(\frac{5}{4}\cdot\log^2 P\right)\cdot(n)$	×	$\mathcal{O}\left(\sqrt{P}\right)$
	2D tile QR binary tree	✓	ScaLAPACK	×	

Performance models of parallel CAQR and ScaLAPACK's parallel QR factorization PDGEQRF on a square $n \times n$ matrix with *P* processors, along with lower bounds on the number of flops, words, and messages. The matrix is stored in a 2-D $P_r \times P_c$ block cyclic layout with square $b \times b$ blocks. We choose b, P_r , and P_c optimally and independently for each algorithm. Everything (messages, words, and flops) is counted along the critical path.

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	2D tile QR flat tree		LAPACK Alg DGEQF	orithm የF	Lower bound
# flops	$\left(rac{4}{3} ight)\cdot\left(n^3 ight)$	✓	$\left(\frac{4}{3}\right)\cdot\left(n^3\right)$	\checkmark	$\mathcal{O}\left(n^{3} ight)$
# words	$3 \cdot \frac{n^3}{\sqrt{W}}$	✓	$\frac{1}{3} \cdot \frac{n^4}{W}$	✓	$\mathcal{O}\left(\frac{n^3}{\sqrt{W}}\right)$
# messages	$12 \cdot \frac{n^3}{W^{3/2}}$	✓	$\frac{1}{2} \cdot \frac{n^3}{W}$	×	$\mathcal{O}\left(\frac{n^3}{W^{3/2}}\right)$
	2D tile QR flat tree	✓	LAPACK	×	

Performance models of sequential CAQR and blocked sequential Householder QR on a square $n \times n$ matrix with fast memory size *W*, along with lower bounds on the number of flops, words, and messages.



$$\begin{split} \mathsf{M}_{\mathsf{fast}} &= 1 \; (\mathsf{MB}) \\ \mathsf{M}_{\mathsf{slow}} &= 1 \; (\mathsf{GB}) \\ \alpha &= 0 \; (\mathsf{SEC}) \\ \beta &= 10^8 \; (\mathsf{GB}/\mathsf{SEC}) \\ \gamma &= 10^{10} \; (\mathsf{GFLOPS}/\mathsf{SEC}) \end{split}$$



2D tile QR - binary tree



- Tile algorithms enable to reduce communication in the sequential case, and in the parallel case wrt existing software
- We can derive communication lower bounds for our problems
- We can attain (polylogarithmically) (assymptotically) communication lower bounds with tile algorithms
- Any tree is possible for the panel factorization
- We (Julien) used tile algorithms to minimize communication,
- We (Emmanuel) now explain them in the context of maximizing parallelism

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- * 70's LINPACK, vector operations: Level-1 BLAS operation
- * 80's LAPACK, block, cache-friendly: Level-3 BLAS operation
- 90's ScaLAPACK, distributed memory:



PBLAS Message passing

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LAPACK QR factorization



- ★ Block algorithm
- \rightarrow (Movie L1)
 - ★ Fork-join parallelism
 - * Multithreaded BLAS

(Movie L4);

LAPACK QR factorization



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LAPACK QR factorization



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LAPACK QR factorization



- ★ Block algorithm
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- ightarrow (Movie L4);

LAPACK QR factorization





- ⋆ Fork-join parallelism
- ★ Multithreaded BLAS

 \rightarrow (Movie L4):



Intel Xeon E7340 quad-socket quad-core (16 cores total)

LAPACK QR factorization



- ★ Block algorithm
- ⋆ Fork-join parallelism
- ★ Multithreaded BLAS

 \rightarrow (Movie L4)

Need for tile algorithms !

Three-layers paradigm

High-level algorithm

2D Tile QR - flat tree

Runtime System

Device kernels	
CPU core	GPU

Tile QR

DAG - 2D tile QR - flat tree



```
for (k = 0; k < TILES; k++) {
    dgeqrt(A[k][k], T[k][k]);
    for (n = k+1; n < TILES; n++) {
        dlarfb(A[k][k], T[k][k], A[k][n]);
    for (m = k+1; m < TILES; n++){
        dtsqrt(A[k][k], A[m][k], T[m][k]);
        for (n = k+1; n < TILES; n++)
        dtsqrtb(A[m][k], T[m][k], A[k][n], A[m][n]);
    }
    }
}</pre>
```

Tile QR

DAG - 2D tile QR - flat tree



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    for (n = k+1; n < TILES; n++) {
        dlarfb(A[k][k], T[k][k], A[k][n]);
    for (m = k+1; m < TILES; n++){
        dtsqrt(A[k][k], A[m][k], T[m][k]);
        for (n = k+1; n < TILES; n++)
        dtsqrtb(A[m][k], T[m][k], A[k][n], A[m][n]);
    }
    }
}</pre>
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    for (m = k+1; m < TILES; m++){
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        for (n = k+1; n < TILES; n++)
        dtsqrtb(A[m][k], T[m][k], A[k][n], A[m][n]);
    }
    }
}</pre>
```

Tile QR

DAG - 2D tile QR - flat tree



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QR Factorization Over Runtime Systems

Tile QR

DAG - 2D tile QR - flat tree



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QR Factorization Over Runtime Systems

Tile QR

DAG - 2D tile QR - flat tree



for (n = k+1; n < TILES; n++)

dssrfb(A[m][k], T[m][k], A[k][n], A[m][n]);

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QR Factorization Over Runtime Systems
DAG - 2D tile QR - flat tree



for (n = k+1; n < TILES; n++)
</pre>

dssrfb(A[m][k], T[m][k], A[k][n], A[m][n]);

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QR Factorization Over Runtime Systems

QR factorization

Tile QR



QR factorization

Tile QR







DAG - 2D tile QR - flat tree



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QR Factorization Over Runtime Systems

DAG - 2D tile QR - flat tree



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QR Factorization Over Runtime Systems



2D tile QR - flat tree - summary

$$\label{eq:FOR_k} \begin{split} & \text{FOR} \; k = 0..TILES-1 \\ & \text{A[k][k], T[k][k]} \leftarrow \text{DGRORT(A[k][k])} \\ & \text{FOR} \; m = k+1..TILES-1 \\ & \text{A[k][k], A[m][k], T[m][k]} \leftarrow \text{DTSORT(A[k][k], A[m][k], T[m][k])} \\ & \text{FOR} \; n = k+1..TILES-1 \\ & \text{A[k][n]} \leftarrow \text{DLARF6d[k][k], T[k][k], A[k][n])} \\ & \text{FOR} \; m = k+1..TILES-1 \\ & \text{A[k][n]} \leftarrow \text{DSSRFB(A[m][k], T[m][k], A[k][n], A[m][n])} \\ & \text{A[k][n]} \leftarrow \text{DSSRFB(A[m][k], T[m][k], A[k][n], A[m][n])} \end{split}$$





- ⋆ Fine granularity;
- ★ Tile layout;
- * Different numerical properties;

★ DAG to schedule.

2D tile QR - flat tree - summary

$$\begin{split} & \text{FOR } k = 0..TILES-1 \\ & \text{A}[k][k], T[k][k] = DGRORT(A[k][k]) \\ & \text{FOR } m = k+1..TILES-1 \\ & \text{A}[k][k], A[m][k], T[m][k]) \leftarrow \text{DTSORT}(A[k][k], A[m][k], T[m][k]) \\ & \text{FOR } n = k+1..TILES-1 \\ & \text{A}[k][n] = DLARFB(A[k][k], T[k][k], A[k][n]) \\ & \text{FOR } m = k+1..TILES-1 \\ & \text{A}[k][n], A[m][n] \leftarrow \text{DSSRFB}(A[m][k], T[m][k], A[k][n], A[m][n]) \end{split}$$





- ⋆ Fine granularity;
- ★ Tile layout;
- * Different numerical properties;
- ★ DAG to schedule.

Outline

1. QR factorization

2. Runtime System for multicore architectures

- 3. Using Accelerators
- 4. Enhancing parallelism
- 5. Distributed Memory

High-level algorithm

2D Tile QR - flat tree

Runtime System

Intrusive (static) scheduler

Device kernels	
CPU core	GPU

Implementation with a static pipeline (Plasma 2.0)



- Work partitioned in one dimension (by block-columns).
- Cyclic assignment of work across all steps of the factorization (pipelining of factorization steps).
- ★ Process tracking by a global progress table.
- * Stall on dependencies (busy waiting).





★ Plasma 1 core

* Plasma 4 cores

Intel Xeon - 16 cores machine

- ★ Node:
 - quad-socket quad-core Intel64 processors (16 cores).
- ★ Intel Xeon processor:
 - quad-core;
 - frequency: 2,4 GHz.
- ★ Theoretical peak:
 - 9.6 Gflop/s/core;
 - 153.6 Gflop/s/node.
- ★ System and compilers:
 - Linux 2.6.25;
 - Intel Compilers 11.0.

Runtime System for multicore architectures

Performance

Intel64-16 cores - QR



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Gflop/s

QR Factorization Over Runtime Systems

IBM Power6 - 32 cores machine

- ★ Node:
 - 16 dual-core Power6 processors (32 cores).
- ★ Power6 processor:
 - dual-core;
 - each core 2-way SMT;
 - L1: 64kB data + 64 kB instructions;
 - L2: 4 MB per core, accessible by the other core;
 - L3: 32 MB per processor, one controller per core (80 MB/s);
 - frequency: 4,7 GHz.
- ★ Theoretical peak:
 - 18.8 Gflop/s/core;
 - 601.6 Gflop/s/node.
- * System and compilers:
 - AIX 5.3;
 - xlf version 12.1;
 - xlc version 10.1.

Runtime System for multicore architectures

Performance

Power6-32 cores - QR



High-level algorithm

Runtime System

DAG vs Fork-Join

A few runtime systems

- * Cilk/Cilk++ [Fork-join];
- ★ SMP Superscalar (SMPSs) [DAG] GPUSs StarSs;
- ★ StarPU;
- * Quark (Plasma, since version 2.1);
- ⋆ DAGuE (dPlasma);
- ★ SuperMatrix;
- * Intel Threading Building Blocks;
- ★ Charm++;
- * ...

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- Intel Threading Building Blocks;
- ★ Charm++;
- * ...

Runtime System for multicore architectures

DAG vs Fork-Join (Kurzak et al.'09)

Fork-Join model - Cilk - 2D

```
cilk void daeart(double *RV1, double *T);
cilk void dtsqrt(double *R, double *V2, double *T);
cilk void dlarfb(double *V1, double *T, double *C1);
void dssrfb(double *V2, double *T, double *C1, double *C2);
cilk void dssrfb (int m, int n, int k)
  dssrfb(A[m][k], T[m][k], A[k][n], A[m][n]);
  if (m == TILES-1 \&\& n == k+1 \&\& k+1 < TILES)
     spawn dgegrt(A[k+1][k+1], T[k+1][k+1]);
  if (n = k+1 \& \& m+1 < T|LES)
     spawn dtsqrt(A[k][k], A[m+1][k], T[m+1][k]);
}
spawn dgegrt(A[0][0], T[0][0]);
sync:
for (k = 0; k < TILES; k++) {
  for (n = k+1; n < TILES; n++)
     spawn dlarfb(A[k][k], T[k][k], A[k][n]);
  if (k+1 < TILES)
     spawn dtsqrt(A[k][k], A[k+1][k], T[k+1][k]);
  sync;
  for (m = k+1; m < TILES; m++) {
     for (n = k+1; n < TILES; n++)
       spawn dssrfb (m, n, k);
     sync;
  }
```



Runtime System for multicore architectures

DAG vs Fork-Join (Kurzak et al.'09)

Fork-Join model - Cilk - 1D

```
void daeart(double *RV1, double *T);
void dtsgrt(double *R, double *V2, double *T);
void dlarfb(double *V1, double *T, double *C1);
void dssrfb(double *V2, double *T, double *C1, double *C2);
cilk void qr panel(int k)
  int m;
  dgegrt(A[k][k], T[k][k]);
  for (m = k+1; m < TILES; m++)
     dtsqrt(A[k][k], A[m][k], T[m][k]);
}
cilk void gr update(int n, int k)
  int m;
  dlarfb(A[k][k], T[k][k], A[k][n]);
  for (m = k+1; m < TILES; m++)
     dssrfb(A[m][k], T[m][k], A[k][n], A[m][n]);
  if (n = k+1)
     spawn gr panel(k+1);
spawn gr panel(0);
svnc:
for (k = 0; k < TILES; k++) {
  for (n = k+1; n < TILES; n++)
     spawn gr update(n, k);
  sync:
```

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DAG - SMPSs

#pragma css task \
 inout(RV1[NB][NB]) output(T[NB][NB])
void dgeqrt(double *RV1, double *T);

#pragma css task \
inout(R[¬], V2[NB][NB]) output(T[NB][NB])
void dtsqrt(double *R, double *V2, double *T);

```
#pragma css task \
    input(V1[\], T[NB][NB]) inout(C1[NB][NB])
void dlarfb(double *V1, double *T, double *C1);
```

```
#pragma css task \
    input(V2[NB][NB], T[NB][NB]) inout(C1[NB][NB], C2[NB][NB])
void dssrfb(double *V2, double *T, double *C1, double *C2);
```

```
#pragma css start
for (k = 0: k < TILES: k++) {</pre>
```

```
dgeqrt(A[k][k], T[k][k]);
```

```
for (m = k+1; m < TILES; m++)
    dtsqrt(A[k][k]\, A[m][k], T[m][k]);</pre>
```

```
for (n = k+1; n < TILE5; n++) {
    diarfb(A[k][k]], T[k][k], A[k][n]);
    for (m = k+1; m < TILE5; m++)
        dssrfb(A[m][k], T[m][k], A[k][n], A[m][n]);
    }
}</pre>
```

```
#pragma css finish
```

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Traces [Kurzak et al.'09]



Performance - Intel 16 cores [Kurzak et al.'09]



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Outline

- 1. QR factorization
- 2. Runtime System for multicore architectures
- 3. Using Accelerators
- 4. Enhancing parallelism
- 5. Distributed Memory

High-level algorithm

Runtime System



High-level algorithm

Runtime System



High-level algorithm

Runtime System



- Kernels for update (ormqr and tsmqr)
 Fully on GPU
- Kernels for panel factorization (geqrt and tsqrt)
 Hybrid implementation CPU + GPU



CUDA tsmqr kernel:

$$\left(\begin{array}{c}A_{ki}^{j}\\A_{mi}\end{array}\right) = \left[I - \left(\begin{array}{c}I\\V_{j}\end{array}\right)T_{j}\left(\begin{array}{c}I\\V_{j}\end{array}\right)^{T}\right]\left(\begin{array}{c}A_{ki}^{j}\\A_{mi}\end{array}\right),$$

1. $D^{1}_{work} = A^{j}_{ki} + V^{T}_{j}A_{mi};$ 2. $D^{2}_{work} = T_{j}D^{1}_{work}; A^{j}_{ki} = A^{j}_{ki} - D^{2}_{work};$ 3. $A_{mi} = A_{mi} - V_{j}D^{2}_{work}.$

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1.
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$$\left(\begin{array}{c}A_{ki}^{j}\\A_{mi}\end{array}\right) = \left[I - \left(\begin{array}{c}I\\V_{j}\end{array}\right)T_{j}\left(\begin{array}{c}I\\V_{j}\end{array}\right)^{T}\right]\left(\begin{array}{c}A_{ki}^{j}\\A_{mi}\end{array}\right),$$

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$$D^{1}_{work} = A^{j}_{ki} + V^{T}_{j}A_{mi};$$

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3. $A_{mi} = A_{mi} - V_{i}D^{2} ...$

- Kernels for update (ormqr and tsmqr)
 Fully on GPU
- Kernels for panel factorization (geqrt and tsqrt)
 Hybrid implementation CPU + GPU



$$\left(\begin{array}{c}A_{ki}^{j}\\A_{mi}\end{array}\right) = \left[I - \left(\begin{array}{c}I\\V_{j}\end{array}\right)T_{j}\left(\begin{array}{c}I\\V_{j}\end{array}\right)^{T}\right]\left(\begin{array}{c}A_{ki}^{j}\\A_{mi}\end{array}\right),$$

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$$D^{1}_{work} = A^{j}_{ki} + V^{T}_{j}A_{mi};$$

2. $D^{2}_{work} = T_{j}D^{1}_{work}; A^{j}_{ki} = A^{j}_{ki} - D^{2}_{work};$
3. $A_{mi} = A_{mi} - V_{i}D^{2}_{mi}.$
GPU kernels

- Kernels for update (ormqr and tsmqr)
 Fully on GPU
- Kernels for panel factorization (geqrt and tsqrt)
 Hybrid implementation CPU + GPU



CUDA tsmqr kernel:

$$\left(\begin{array}{c}A_{ki}^{j}\\A_{mi}\end{array}\right) = \left[I - \left(\begin{array}{c}I\\V_{j}\end{array}\right)T_{j}\left(\begin{array}{c}I\\V_{j}\end{array}\right)^{T}\right]\left(\begin{array}{c}A_{ki}^{j}\\A_{mi}\end{array}\right),$$

1.
$$D^{1}_{work} = A^{j}_{ki} + V^{T}_{j}A_{mi};$$

2. $D^{2}_{work} = T_{j}D^{1}_{work}; A^{j}_{ki} = A^{j}_{ki} - D^{2}_{work};$
3. $A_{mi} = A_{mi} - V_{i}D^{2}_{mi}.$

Architecture

- $\star\,$ AMD Opteron 8358 SE CPU, 4 \times 4, 2.4GHz, 4 $\times\,$ 8GB
- \star NVIDIA Tesla S1070 GPU, 4 \times 240, 1.3GHz, 4 \times 4GB
- ★ single precision:
 - peak: 3067Gflop/s (307.2 + 2760)
 - sgemm: 1908Gflop/s (256 + 1652)
- double precision:
 - peak: 498.6Gflop/s (153.6 + 345)
 - dgemm: 467.2Gflop/s (131.2 + 336)

Tuning



ib:

32

64

7-96

128

192

₩ 224

× 256

Performance



Performance



Three-layers paradigm

High-level algorithm

Runtime System				
StarPU				
Device kernels				
CPU core	GPU			

GPU-enabled runtime systems

- ★ Cilk/Cilk++;
- * SMP Superscalar (SMPSs) GPUSs StarSs;
- ⋆ StarPU;
- * Quark (Plasma, since version 2.1);
- ⋆ DAGuE (dPlasma);
- ★ SuperMatrix;
- Intel Threading Building Blocks;
- ★ Charm++;
- * ...

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- ★ SuperMatrix;
- Intel Threading Building Blocks;
- ★ Charm++;
- * ...

The StarPU runtime system [Augonnet et al.]

- Data management:
 - Checks dependences;
 - Ensures coherency;
- ★ Supports:
 - SMP/Multicore Processors (x86, PPC, ...);
 - NVIDIA GPUs;
 - OpenCL devices;
 - Cell Processors (experimental).
- * Scheduling module.



2D Tile QR - flat tree - over StarPU

for (k = 0; k < min(MT, NT); k++) { starpu_Insert_Task(&cl_zgeqrt, k , k, ...);

for (n = k+1; n < NT; n++)starpu_Insert_Task(&cl_zunmqr, k, n, ...);

```
for (m = k+1; m < MT; m++) {
  starpu Insert Task(&cl ztsgrt, m, k, ...);
```

for (n = k+1; n < NT; n++)starpu Insert_Task(&cl_ztsmqr, m, n, k, ...);

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2D Tile QR - flat tree - over StarPU

for (k = 0; k < min(MT, NT); k++) { starpu_Insert_Task(&cl_zgeqrt, k , k, ...);

```
for (n = k+1; n < NT; n++)
  starpu Insert Task(&cl zunmgr, k, n, ...);
```

```
for (m = k+1; m < MT; m++) {
  starpu Insert Task(&cl ztsgrt, m, k, ...);
```

```
for (n = k+1; n < NT; n++)
  starpu Insert_Task(&cl_ztsmqr, m, n, k, ...);
```

See code

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Using Accelerators

StarPU

Relieving anti-dependencies (SMPSs trick reminder)

#pragma css task \
 inout(RV1[NB][NB]) output(T[NB][NB])
void dgeqrt(double *RV1, double *T);

#pragma css task \
 inout(R[¬], V2[NB][NB]) output(T[NB][NB])
void dtsqrt(double *R, double *V2, double *T);

#pragma css task \
 input(V1[\], T[NB][NB]) inout(C1[NB][NB])
void dlarfb(double *V1, double *T, double *C1);

```
#pragma css task \
    input(V2[NB][NB], T[NB][NB]) inout(C1[NB][NB], C2[NB][NB])
void dssrfb(double *V2, double *T, double *C1, double *C2);
```

```
#pragma css start
for (k = 0: k < TILES: k++) {</pre>
```

```
dgeqrt(A[k][k], T[k][k]);
```

```
for (m = k+1; m < TILES; m++)
    dtsqrt(A[k][k]\, A[m][k], T[m][k]);</pre>
```

```
for (n = k+1; n < TILE5; n++) {
    dlarfb(A[k][k]], T[k][k], A[k][n]);
    for (m = k+1; m < TILE5; m++)
    dssrfb(A[m][k], T[m][k], A[k][n], A[m][n]);
}</pre>
```

```
#pragma css finish
```



Using Accelerators

StarPU

Relieving anti-dependencies (using StarPU)

GFlop/s











Impact of the scheduling policy



Name	Folicy description		
heft-tmdp-pr	heft-tmdp with data PRefetch		
heft-tmdp	heft-tm with remote Data Penalty ($\alpha T_{data \ transfert} + T_{computation}$)		
heft-tm-pr	heft-tm with data PRefetch		
heft-tm	HEFT based on Task duration Models ($T_{data \ transfert} + T_{computation}$)		
greedy	Greedy policy		

Nome



Using Accelerators

StarPU

Impact of the Data Penalty on the total amount of data movement



Matrix order	9600	24960	30720	34560
heft-tmdp-pr	1.9 GB	16.3 GB	25.4 GB	41.6 GB
heft-tm-pr	3.8 GB	57.2 GB	105.6 GB	154.7 GB

Performance



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Performance



+ 200Gflop/s but 12 cores = 150Gflop/s

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Heterogeneity

Kernel	CPU	GPU	Speedup
sgeqrt	9 Gflops	60 Gflops	≈6
stsqrt	12 Gflops	67 Gflops	≈6
sormqr	8.5 Gflops	227 Gflops	≈27
stsmqr	10 Gflops	285 Gflops	≈27

* Task distribution observed on StarPU:

- sgeqrt: 20% of tasks on GPUs
- stsmqr: 92.5% of tasks on GPUs
- * Taking advantage of heterogeneity !
 - Only do what you are good for
 - Don't do what you are not good for

Outline

- 1. QR factorization
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DAG of a 4x4 tile matrix



2D tile QR - hybrid binary/flat tree



DAG of a 4x4 tile matrix

2D tile QR - flat tree



2D tile QR - hybrid binary/flat tree



Enhancing parallelism

2D tile QR - hybrid binary/flat tree

First panel factorization and corresponding updates.





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QR Factorization Over Runtime Systems

Enhancing parallelism

2D tile QR - hybrid binary/flat tree

Second panel factorization and corresponding updates.





Enhancing parallelism

2D tile QR - hybrid binary/flat tree

Final panel factorization.





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QR Factorization Over Runtime Systems

Enhancing parallelism

2D tile QR - hybrid binary/flat tree

Final panel factorization.





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QR Factorization Over Runtime Systems

Enhancing parallelism

16x2 tile matrix - 1 domain (flat tree)



Enhancing parallelism

16x2 tile matrix - 8 domains (hybrid tree)



Enhancing parallelism

16x2 tile matrix - 16 domains (binary tree)



Enhancing parallelism

32x4 tile matrix - 1 domain (flat tree)



Enhancing parallelism

32x4 tile matrix - 16 domains (hybrid tree)


Enhancing parallelism

Enhancing parallelism

32x4 tile matrix - 16 domains (hybrid tree)



Traces (8 cores)

N = 400 - 16 cores



M = 6400 - 16 cores



$M = 51200 - 200 \le N \le 3200$



Heterogeneous platform - double precision - N = 2*960



Outline

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Distributed Memory

Scalability - Cholesky 6 nodes ; 3 GPUs and 12 cores per node



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QR Factorization Over Runtime Systems

Distributed Memory

Scalability - Cholesky Total of 3 GPUs and 12 cores



129

Distributed Memory

Scalability: towards exascale ?



Conclusion

- ★ three-layers paradigm;
- * productivity and performance portability;
- * Cholesky, (CA-)QR and LU solvers;
- * to be released into the MAGMA library.

Perspectives

- high-level complex routines (eigensolvers, sparse solvers, ...)
- scalable runtime;
- high-performance kernels;
- * Autotuning framework;
- Clever scheduling algorithms;



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<u> [hanks</u>]

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Thanks!

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* Thanks!

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Thanks!

* . . .