SEMINAIRE MATHEMATIQUE-INFORMATIQUE

Projet SAFIR
UNSA - INRIA - CNRS :
«*Systèmes Algébriques Formels pour l'Industrie et la Recherche* »

Lieu: *INRIA*,
2004, route des Lucioles,
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Salle E003.
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Le vendredi 12 Juillet à 14 heures, salle E003 :

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«*Symbolic Modelling in Circuit Simulation* »

Simulation has a growing importance in industrial production since many years. Corresponding to faster changing product cycles, new and more complicated simulation models have to be developed in a shorter time. In the field of circuit simulation, models for MOS transistors are of special interest. Because of the nonlinearity of the transistor functions with respect to the input drain and voltages and because of the coupling of the transistor to the entire simulation system, furthermore the derivatives of these transistor functions are needed.

There are many different ways for implementing the functional description of a simulation model followed by an (automatically executed) additional development and implementation of the derivatives of the mathematical model. In this talk, the application of the ADIFOR tool for the automatic differentiation of a Fortran code as well as corresponding results will be shown. Starting on a higher level, the mathematical description of the functions itsself, the application of a SYPERB tool as well as of the well-known MAPLE tool to the MOS Equations is discussed. The SYPERB system with an operator based notation using the programming language C++ and LEX and YACC tools enables not only reading, creating and evaluation of the mathematical formulas but also the differentiation with different kinds of arithmetics (e.g. interval arithmetic) and both forward or the reverse mode of automatic differentiation. In contrast to SYPERB, MAPLE uses the symbolic mode of differentiation, furthermore it enables the automatic generation of FORTRAN text or the graphical representation for a given mathematical function (besides other features).

Results concernig the process of modelling itself as well as concerning the execution speed will be shown for the application to MOS transistor models.