

Liste of publications

Jean-Vivien Millo

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References

PhD thesis

- [1] Jean-Vivien Millo. *Ordonnancements périodique dans les réseaux de processus: application à la conception insensible aux latences*. PhD thesis, AOSTE Project, INRIA Sophia-Antipolis and University of Nice Sophia-Antipolis, Nice, France, 2008.

International peer reviewed journals

- [2] Jean-Vivien Millo and Robert Simone. Explicit routing schemes for implementation of cellular automata on processor arrays. *Natural Computing*, 12(3):353–368, 2013.
- [3] Jean-Vivien Millo and Robert de Simone. Periodic scheduling of marked graphs using balanced binary words. *Theoretical Computer Science*, 458:113–130, November 2012.
- [4] Calin Glitia, Julien DeAntoni, Frédéric Mallet, Jean-Vivien Millo, Pierre Boulet, and Abdoulaye Gamatié. Progressive and explicit refinement of scheduling for multidimensional data-flow applications using uml marte. *Design Automation for Embedded Systems*, 16:137–169, 2012. 10.1007/s10617-012-9093-y.
- [5] Julien Boucaron, Robert de Simone, and Jean-Vivien Millo. Formal methods for scheduling of latency-insensitive designs. *EURASIP J. Embedded Syst.*, 2007(1):8–8, January 2007.

International peer reviewed conferences

- [6] Frederic Mallet, Jean-Vivien Millo, and Robert de Simone. Safe ccsl specifications and marked graphs. In *Formal Methods and Models for Codesign (MEMOCODE), 2013 Eleventh IEEE/ACM International Conference on*, pages 157–166, 2013.
- [7] Frdric Mallet and Jean-Viven Millo. Boundness issues in ccsl specifications. In Lindsay Groves and Jing Sun, editors, *Formal Methods and Software Engineering*, volume 8144 of *Lecture Notes in Computer Science*, pages 20–35. Springer Berlin Heidelberg, 2013.
- [8] Arda Goknil, Ivan Kurtev, and Jean-Vivien Millo. A metamodeling approach for reasoning on multiple requirements models. In *IEEE International EDOC Conference*, Vancouver, Canada, September 2013.
- [9] Jean-Vivien Millo, S Ramesh, S Krishna, and Ganesh Narwane. Compositional verification of software product lines. In *Integrated Formal Methods, (iFM), Turku, Finland*, 2013.
- [10] Swarup Mohalik, S. Ramesh, Jean-Vivien Millo, Shankara Narayanan Krishna, and Ganesh Khandu Narwane. Tracing spls precisely and efficiently. In *Proceedings of the 16th International Software Product Line Conference - Volume 1, SPLC '12*, pages 186–195, New York, NY, USA, 2012. ACM.

- [11] Jean-Vivien Millo, Swarup K. Mohalik, and S. Ramesh. Integrated analysis of software product lines: a constraint based framework for consistency, liveness, and commonness checking. In *Proceedings of the 4th India Software Engineering Conference, ISEC '11*, pages 41–50, New York, NY, USA, 2011. ACM.
- [12] Julien Boucaron, Jean-Vivien Millo, and Robert de Simone. Latency-insensitive design and central repetitive scheduling. In *MEMOCODE '06. Proceedings. Fourth ACM and IEEE International Conference on Formal Methods and Models for Co-Design, 2006.*, pages 175– 183, Piscataway, NJ, USA, 2006. IEEE Press.

International invited journal

- [13] Jean-Vivien Millo, Frdric Mallet, Anthony Coadou, and S. Ramesh. Scenario-based verification in presence of variability using a synchronous approach. *Frontiers of Computer Science*, 7(5):650–672, 2013.

Workshops

- [14] Jean-Vivien Millo and Ramesh S. Relating requirement and design variabilities. In *Proceedings of the international workshop on Software Quality and Management (SQAM'12)*, December 2012.
- [15] Jean-Vivien Millo and Robert de Simone. Refining cellular automata with routing constraints. In Enrico Formenti, editor, *Automata & JAC (Exploratory track)*, volume 2, September 2012.
- [16] Julien Boucaron and Jean-Vivien Millo. Compositionality of statically scheduled ip. *Electron. Notes Theor. Comput. Sci.*, 200:71–87, February 2008.
- [17] Julien Boucaron, Jean-Vivien Millo, and Robert De Simone. Another glance at relay stations in latency-insensitive design. *Electron. Notes Theor. Comput. Sci.*, 146:41–59, January 2006.

Miscellaneous

- [18] Jean-Vivien Millo, Julien Boucaron, and Robert De Simone. Latency insensitive design : Dynamic and static scheduling with proper formal devices. In *SAME'06*, Sophia-Antipolis, France, 2006. SAME.