Jean-Vivien Millo
PhD in Computer Science and Embedded System

31 years old - (+33)603563330 - jvmillo@gmail.com

I'm an R&D engineer with 9 years of experience specialized in analysis, verification and design of embedded systems, including 2,5 years in India. I'm searching for an engineering position where my skills and experiences will benefit innovative projects in the context of international collaborations.

Skills

Areas of expertise:	High level modeling of embedded and real-time system, Platform based design Y-chart, Model based design, Algorithms, Design patterns , Multithreading Compiler and code optimization, SoC design, Scheduling, Synchronous languages Verification and validation of hardware/ software design, Concurrency theory Models of computation and communication, Software product line (Variability)
Standards and Languages:	*from high proficiency to low proficiency* Java, C, Linux system (scripting, programming), C++, Matlab SL/SF, SCADE Eclipse (EMF), SVN (GIT), Promela/SPIN, Yices, nuSMV LaTeX, Hardware architecture, GPGPU, System C, UML Marte, AUTOSAR CUDA, OpenCL, OpenMP, MPI, SQL (Oracle), HTML, Networking
Professional skills	Project management, Team working, International collaboration (Small) Team management, Training, Reviewing external work Technical presentation and communication (writing and oral)
Languages:	English: Fluent French: Mother tong
Sports:	Climbing, Hiking, Volley ball, Basket ball

Diplomas

2008	PhD degree on computer science and embedded systems	Univ. of Nice Sophia-Antipolis, France
2005	Engineering degree on embedded systems and telecom.	ESIGETEL, Avon, France
2005	MSc degree on theoretical and applied computer science	Univ. of Marne La Vallée, France
2003	BSc degree on computer science	Univ. of Marne La Vallée, France
2002	French academic DUT on computer science	Univ. of Nice Sophia-Antipolis, France
2000	French Baccalaureate in science (high school diploma)	LEGTA-H, Antibes, France

Work experience

2011 - 2014	R&D engineer	AOSTE team, INRIA Sophia-Antipolis, France	(3 years)
	↳ *Project 1:*	*Application Architecture Adequation*	
	↳ *Project 2:*	*Static routing for network on chip*	
2011 - 2014	Teaching Vacation	Univ. of Nice Sophia Antipolis, France	(400 hours)
	↳ See related section		
2009 - 2011	R&D engineer	India Science Lab, GM R&D, India	(2.5 years)
	↳ *Project 3:*	*Formal verification of features interactions*	
2005 - 2008	MSc & PhD candidate	AOSTE team, INRIA Sophia-Antipolis, France	(4 years)
	↳ *Project 4:*	*KPassa: formal analysis of data-flow application*	

Management

- 1 PhD student (April 2013 -)
- 1 Master student for a 1 year internship (Sept 2012 - Sept 2013)
- 2 Master students for a short term internship (2011)
- 2 Master students for a short term internship (2010) [when I was in General Motors India]

Participation to international collaboration

- 2009 - 2014: Collaboration with IIT-Bombay, India and General Motors USA *as leader*
- 2012 - 2013: Collaboration with University of Sevilla, Spain *as participant*
- 2013- 2014: Collaboration with ISTI, CNR, Pisa, Italia *as participant*
- 2013- 2014: Collaboration with Technische Universiteit Eindhoven, The Netherlands *as participant*

Teaching activities

My teaching activity took place at the University of Nice Sophia-Antipolis in the department of computer science.

Teaching duty 2011-12: 105 hours
Teaching duty 2012-13: 100 hours
Teaching duty 2013-14: 192 hours.

- Programmation orientée objet, Master MIAGE 1 2011-12, 2012-13, 2013-14
- Concurrency and Parallelism, Master 1 International 2012-13, 2013-14
- Langage et Automate, Licence 3 Info, 2011-12
- Programmation Web, DUT Informatique, 2011-12
- Introduction aux Bases de Données, Licence 2 Info, 2011-12
- Formal Models for Network-on-Chips, Master 2 International, 2011-12/ 2012-13/ 2013-14
- Systèmes distribués, Master 1 MIAGE, 2012-13
- Système et réseaux, Licence 3 MIAGE, 2013-14
- Base de données, Licence 3 MIAGE, 2013-14
- Systèmes d'exploitation, Licence 1 Informatique 2012-13/2013-14
- Programmation Orientée objet, Licence 3 MIAGE, 2013-14
- Formalismes pour l'analyse fonctionnelle et temporelle, Master 2 Info, 2013-14
- Patrons de conception, Master 1 MIAGE, 2013-14

References

Robert de Simone, Directeur de recherche, INRIA Sophia-Antipolis
robert.de_simone@inria.fr

S. Ramesh, Technical Fellow, General Motors R&D, Warren, USA
ramesh.s@gm.com

Frédéric Mallet, Vice-director of the computer science department, Univ. Nice Sophia-Antipolis
Frederic.Mallet@unice.fr

Jean-Vivien Millo
PhD in Computer Science and Embedded System

31 years old - (+33)603563330 - jvmillo@gmail.com

Project 1: Application architecture adequation (2014)

The goal of this project is to define methods, algorithms and tools to automate the allocation of applications on embedded platforms (architectures). We restrict ourselves to *data flow* applications and will focus on Network-on-chip based architectures.

Achievements:

- Definition of the high level models of the application, the architecture and the allocation.
- Definition of the allocation methodology.
- Validation of the approach on a case study

Deliverables:

- The Ecore models of the application, the architecture and the allocation along with the model transformation toward analysis and scheduling tool such as KPassa.
- A scientific publication.

About the project:

- My role: Technical lead.
- Number or participants: 6

Project 2: Static routing for network on chip (2013)

The goal of this project is to define a routing pattern to optimize the usage of a Network on Chip and avoid congestion. Static routing is relevant when the application (the one mapped on the NoC based embedded device) is of the class of *data flow* because the flows of data are known at compile time and so they can be analysed.

Achievements:

- Definition of a data flow process network to model the application.
- Definition of the routing algorithm.
- Validation of the model and the algorithm on a FFT case study

Deliverables:

- A System C model of a 2D network on chip with special focus on the routers as programmable elements.
- Three scientific publications.

About the project:

- My role: Technical lead.
- Number or participants: 3

Project 3: Formal verification of features interactions (2011)

A software product line is a development paradigm where a family of closely related software products are developed altogether. The set of features is common to the family but every product incorporates its own subset. The features are thus developed once for all and composed. The problem of features interaction is that even though two features work fine separately, their composition raises unexpected behaviors.

We have proposed a formal verification approach that checks the interactions between a limited amount of features against scenarios.

Achievements:

- Definition of a scenario language and its translation into an observer.
- Definition of a verification flow based on existing verification languages and tools.

Deliverables:

- A verification flow involving EMF technologies, the Esterel compiler (v5.92), and the Xeve verification environment.
- A scientific publications.

About the project:

- My role: Technical lead.
- Number or participants: 4

Project 4: KPassa, formal analysis of data-flow application (2008)

KPassa is a JAVA based tool made to analyze and schedule *data flow* applications.

Achievements:

- Definition of a scheduling algorithm that optimize the throughput and minimize the need for communication buffers.

Deliverables:

- A tool available online at http://www-sop.inria.fr/members/Jean-Vivien.Millo/kpassa.
- Six scientific publications.

About the project:

- My role: Technical lead.
- Number or participants: 7 but maximum 3 simultaneously