Application Architecture Adequacy through an FFT case study

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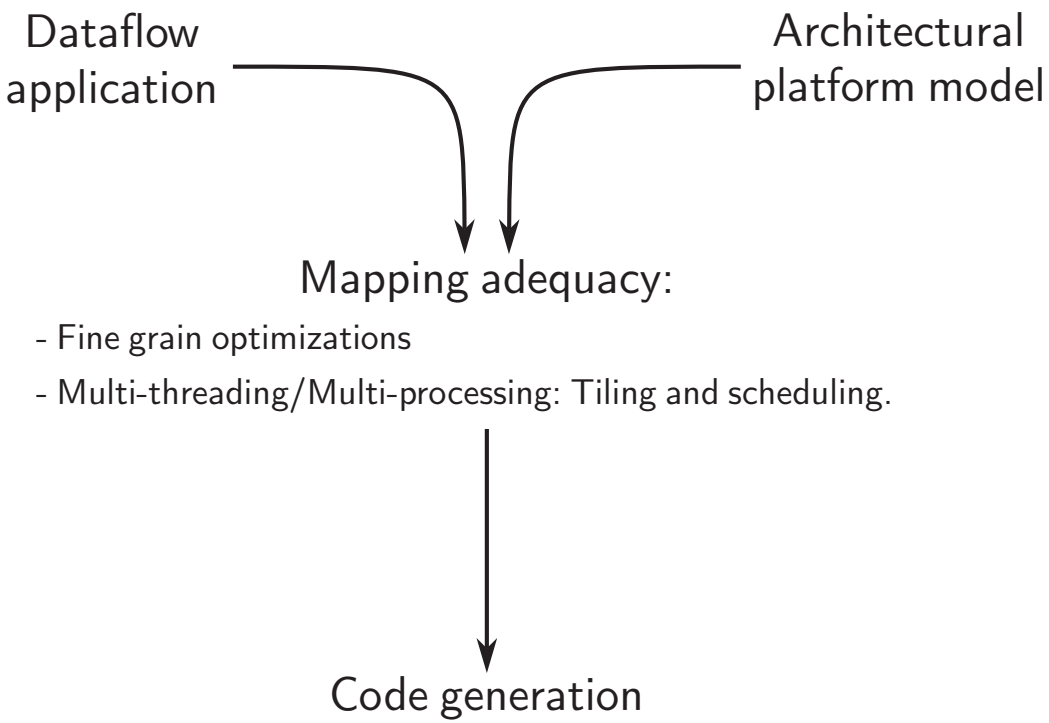
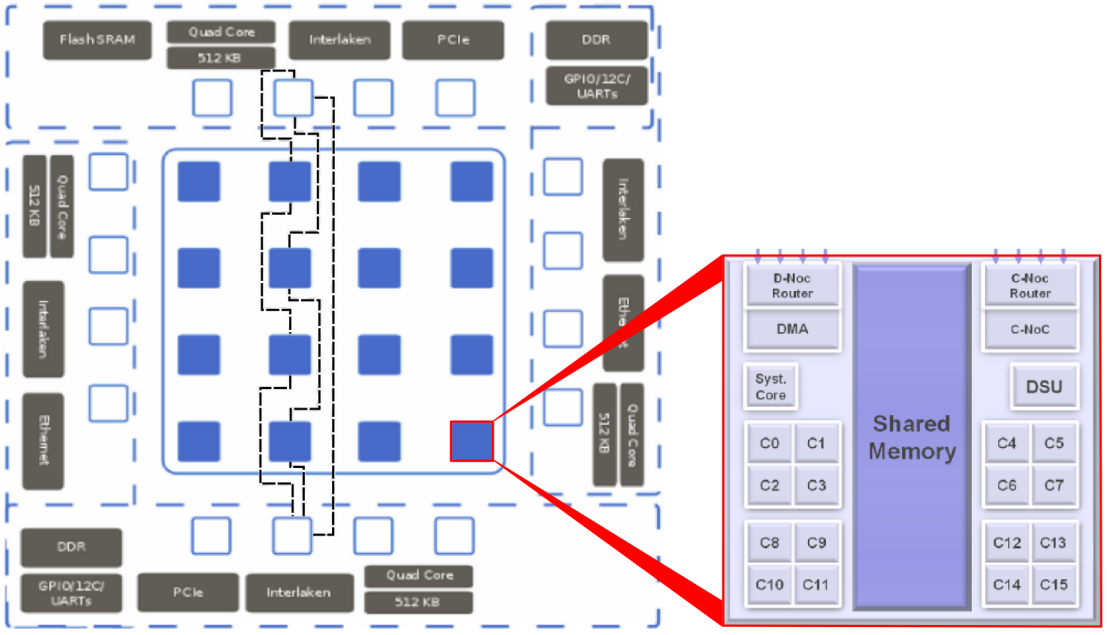
Problem: Weak portability for a given application.

AAA:



AAA requires a description of the HW (memory hierarchy, interconnect, computing elements, ...).

Motivations - Modeling - Limitations



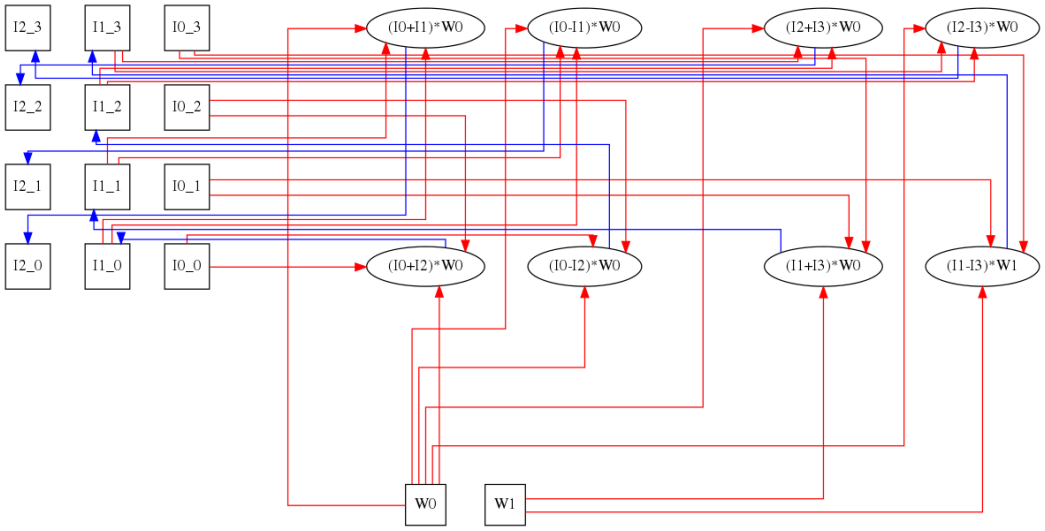
Kalray MPPA256

- Networks on chips replace/complement buses (for scalability purposes).
- Many different NoC based platforms exist.
- GPUs and CPUs have heterogeneous programming models.

Required steps for AAA:

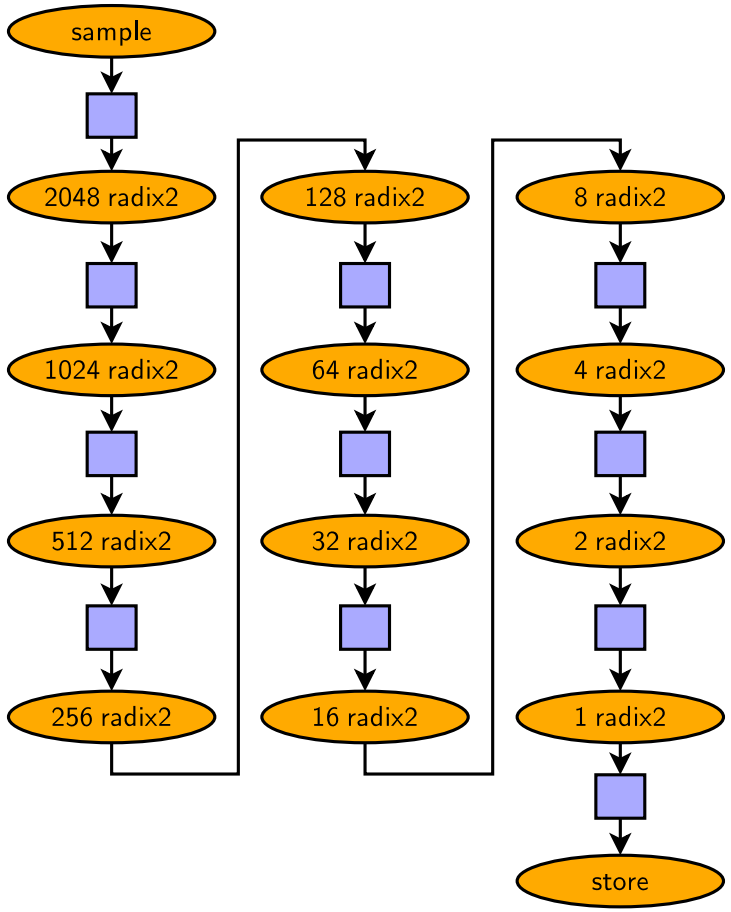
1. **Dataflow SW modeling**: architecture independent
2. **Hardware modeling**
3. **Fine grain adaptation** (ILP) for each computation unit
4. **Tiling and mapping** coarse grain parallelism
5. **Scheduling** computation **and** communication

Dataflow process networks: fine grain parallelism



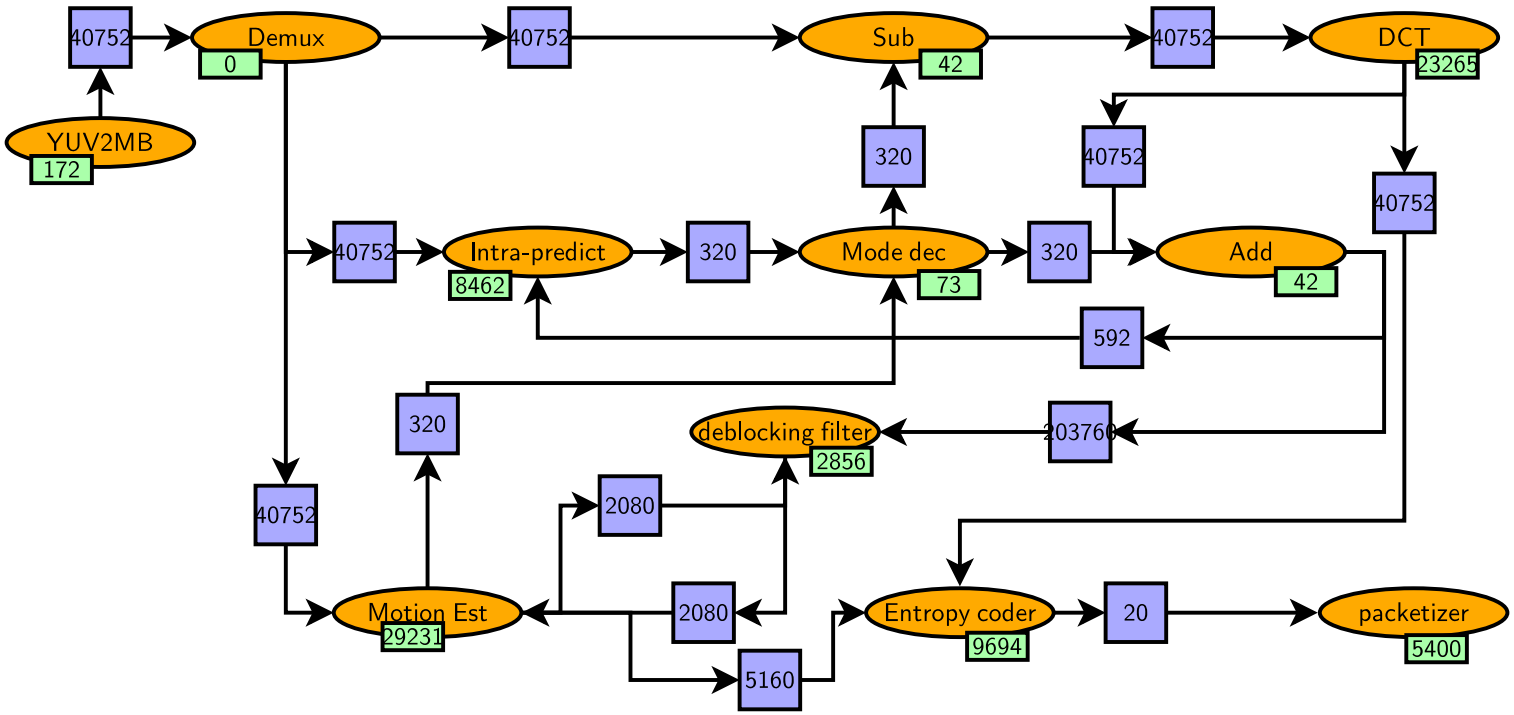
4-samples FFT Data Flow representation

Dataflow process networks: coarse grain parallelism



Coarse 4096-samples FFT Data Flow representation

Dataflow process networks: refined application



H264 encoding annotated Data Flow representation

- Sparse compiler parameters: streamIt
- Sparse code annotation: openMP (nb of threads), openCL (clDevice class), cuda (cudaDeviceProp structure).
- High level descriptions: sysML, TLM systemC
- Very accurate descriptions: Cycle Accurate Bit Accurate SystemC
- Synthesizable descriptions: HDL languages

AAA requires a hardware description: nb of threads and which address space they share, cache sizes, nb of DMA engines, throughput/latency/routing of the **interconnect**.

The AAA methodology is required for efficient design ans portability.

Going further: Consider all non-functional properties (Temperature/Power/Performance).

Limitations: It is much harder to model dynamic behaviors with dataflow process networks (data-dependent execution, temperature/power thresholds). HOPE (Hierarchically Organized Power/Energy management).

http://anr-hope.unice.fr/.