# watchdog

Designed with syncCharts 2.084

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This report has been generated by `syncCharts v2.084`. SyncCharts has been created and developed by Charles André, I3S Lab. - University of Nice (F)
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## Comments

```
Watchdog
   This is an example of pure esterel program.
   Basically it's a SR flip-flop (set and reset inputs).
   When ON, if more than 5 occurrences of 'top' occur then
the system goes to an 'alarm' state.  'reset' must occur
to get out this state.
   This example illustrates:  hierarchy, parallelism, preemption
and normal termination (see module 'timer' and its final
stars).
```

# Chapter 1

# Modules

## 1.1 Tree

Table 1.1:  Application Tree

| Tree | |
|------|---|
| (p.6) | watchdog |
| (p.4) | control |
| (p.3) | timer |

## 1.2 timer
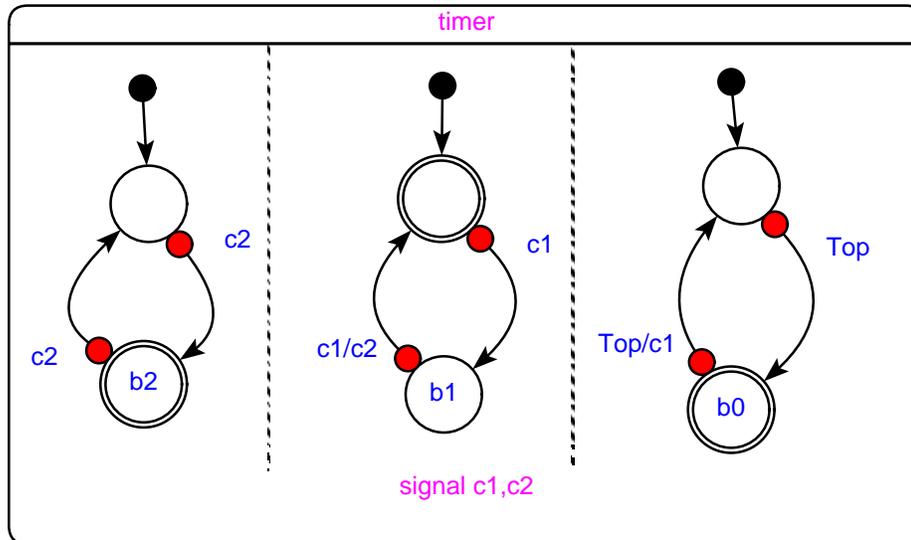


Figure 1.1: Macro-state timer

## Declarations

Table 1.2:  Declarations

| Declarations |
| --- |
| input Top; |
| output b1; |
| output b0; |
| output b2; |

## 1.3   control
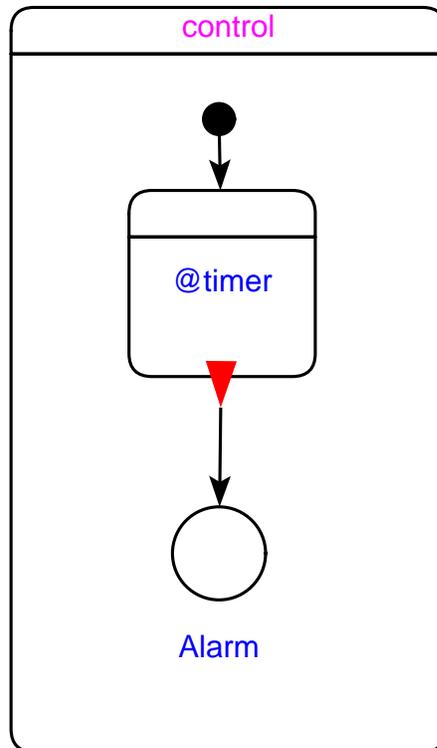


Figure 1.2: Macro-state `control`

**Declarations**

Table 1.3:   Declarations

| Declarations |
|---|
| input Top; |
| output Alarm; |
| *continued on next page* |

```
output b1;
output b0;
output b2;
```

## 1.4   watchdog
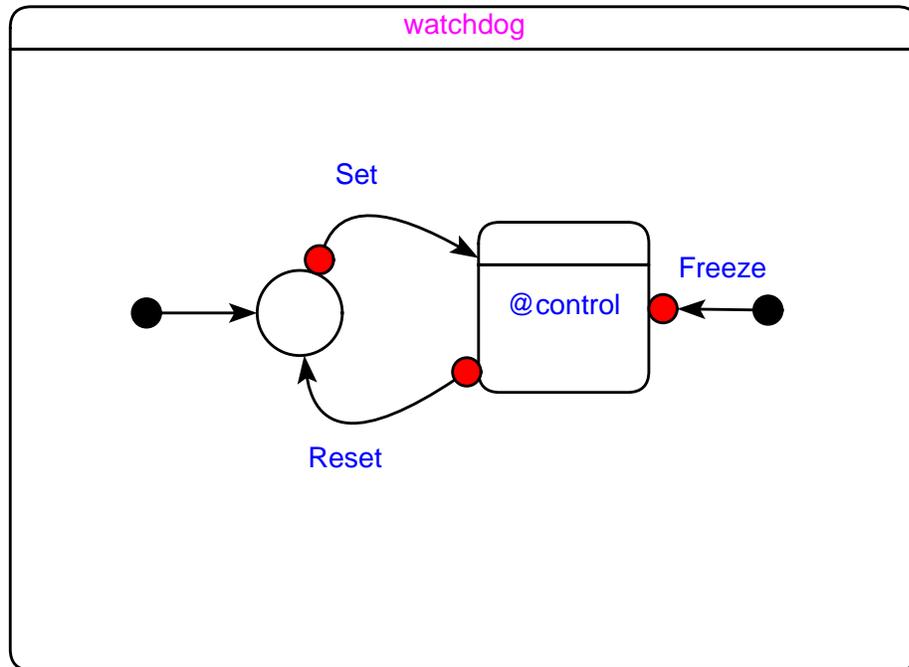


Figure 1.3: Macro-state watchdog

## Declarations

Table 1.4:  Declarations

| Declarations |
| --- |
| input Freeze; |
| input Set; |
| input Reset; |
| input Top; |
| *continued on next page* |

```
continued from the previous page
output Alarm;
output b1;
output b0;
output b2;
```

## 1.5   External Declarations

Declarations to be provided by the host language:

# Chapter 2

# Other Views