UML MARTE Time Model for SPIRIT IP-XACT

Aamir Mehmood Khan, Frédéric Mallet, Charles André, Robert de Simone
Projet AOSTE (INRIA & I3S/CNRS, Sophia Antipolis)

Objective:
Early functional or extra-functional validation/analysis of systems of IPs within UML. This framework must use IP-XACT IP metadata interchange format.

Overview:
- Use the SPIRIT IP-XACT to build a UML sub-profile, thus using the Model Driven Engineering (MDE) approach to provide gateways between UML and SPIRIT. The result helps to represent IP structural information at much higher levels of abstraction.
- Verify and validate the IP timing characteristics at various abstraction levels using the test benches. These test benches simulate timing patterns and compare their results as different abstraction levels.
- Represent the timing characteristics or the behavior of a system/IP in textual form using the constraints defined in CCSL. These constraints can then be attached to the existing IP-XACT components to represent behavior.

Terminologies:
Unified Modeling Language: UML is a general purpose modeling language that can be adapted to specific domains using semantic variation points and profiles.
MARTE UML Profile: Profiles in the UML are a generic extension mechanism for building UML models in particular domains. It adds capabilities to UML for model-driven development of Real Time and Embedded Systems (RTES).
Intellectual Property: IP is a broad category of materials that are legally recognized as proprietary assets of an organization.
IP-XACT: IP-XACT defines and describes electronic components and their designs. SPIRIT Consortium proposed the IP-XACT standard as a mean for describing and handling intellectual property enabling automated configuration and integration through tools.
SystemC/VHDL: SystemC is a programming language used for design and simulation of systems at higher abstraction levels (TLM/CP). VHDL is used to design and simulate electronic systems at the much lower levels like RTL.
ATLAS Transformation Language: ATL is a model transformation language which provides ways to produce a set of target models from a set of source models.
Clock Constraint Specification Language: CCSL allows the representation of clocks or timing specifications in textual form. These constraints can be used later to reproduce the waveforms using Time-Square software.

Tools used:
- Magic Draw, Papyrus UML, IBM RSA (Rational Software Architecture), Esterel, ModelSim VHDL, SystemC 2.0 with TLM 2, ATL, CCSL, Time Square, XML, XSLT.

Literature cited:
- UML MARTE Time Model for SPIRIT IP-XACT, ACM TECS Journal September, 08. Khan, A. M., Mallet, F., Andre, C., and de Simone, R.
- Holistic system modeling and refinement of interconnected microelectronics systems. DATE’08. Zimmermann, J., Bringmann, O., Gerlach, J., Schaefer, F., and Nageldinger, U.