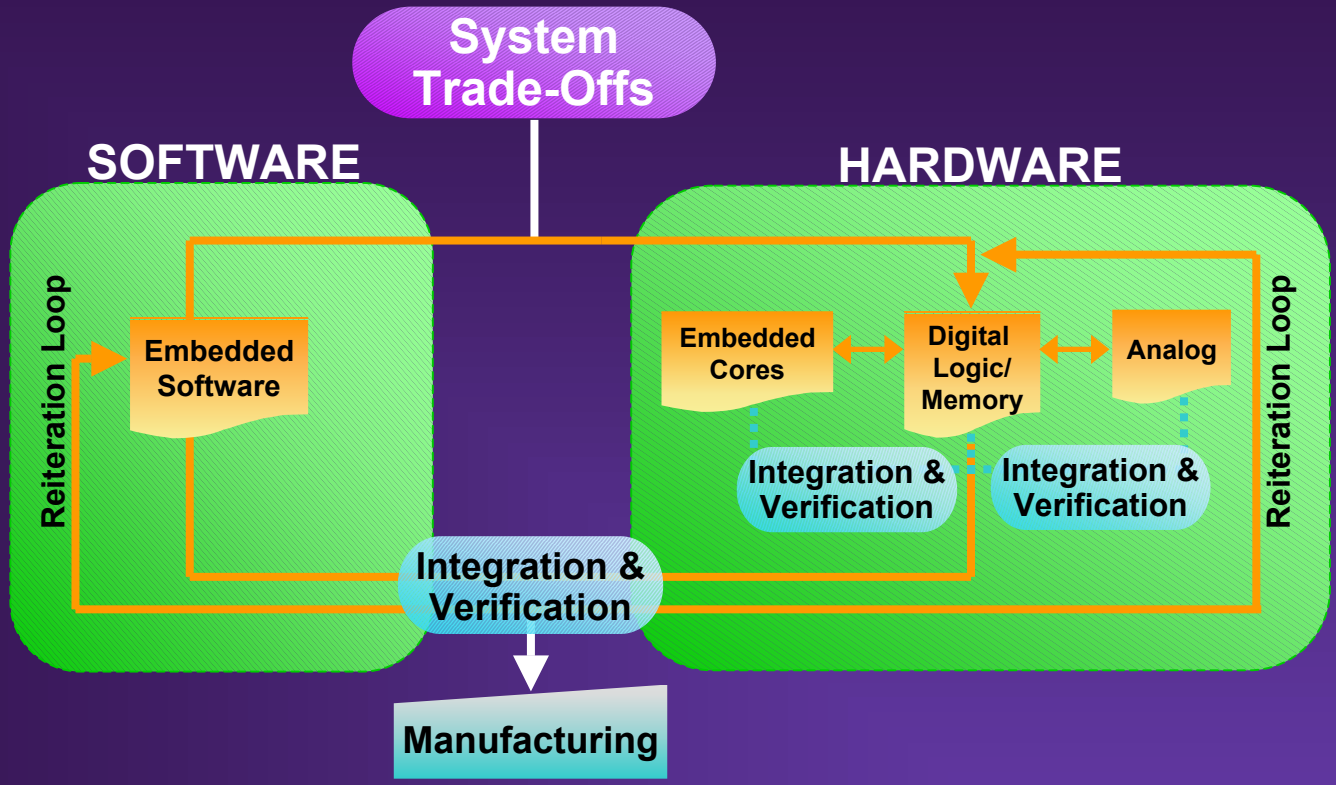
Who drives SoC Chips:Applications or Silicon ?

Pierre Bricaud
Director, R&D Solutions Group
Synopsys, Inc.
Sophia Antipolis

SoC is not just HW, its HW+SW+Application



- Multiple Technologies - Hardware/Software, Analog/Digital
- Multiple Teams - Hardware (Analog/Digital), Software, System
- Multiple Embedded Systems - IP Cores

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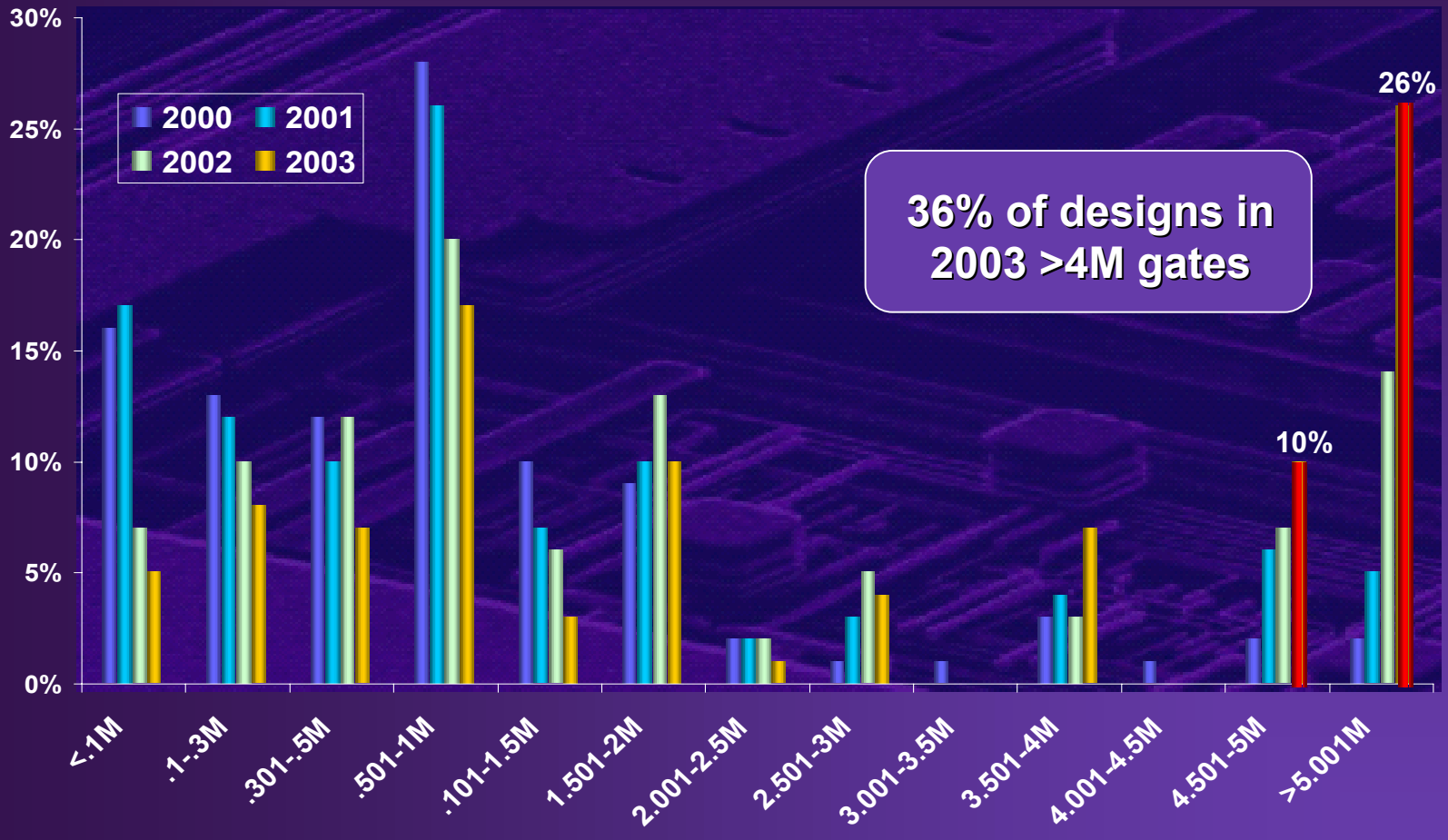
Average Gate Count Continues to Grow



Data from Synopsys SNUG San Jose 2003 seminar survey

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Design Keeps Getting More Complex

		180nm	130nm	90nm	65nm
Computing	Parallelism				
	64 Bits				
IP	IP	30%	50%	70%	90%
Flow	Hierarchy	Large designs			
	Database	Partial	Partial	Integrated	Integrated
	API	Proprietary	Open	Open	Open
S, P&R	S, P&R	S&P - R	S&P - R	Integrated	Integrated
	Handoff	Placed Gates	Placed Gates	Layout	Layout
Timing	TC				
	SI				
	L for Busses		1.5GHz	1.5GHz	1.5GHz
Clocking	Cycles across Chip	1	Few	Few	Many
	Clocking	Sync	Sync	Sync/Async	Sync/Async
	IR drop	Power	Power	Power	Power&Signal

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Design Keeps Getting More Complex

		180nm	130nm	90nm	65nm
Power	Clock Gating				
	Multi Vdd				
	Multi Vth (leakage)				
Test	Scan				
	Mem Bist				
	Logic Bist				
	Design for Debug				
RET	OPC				
	PSM				
	DR for RET				
DFM	Statistical Timing				
	PD for DFM				
Analog	P&R	Manual	Semi-Auto	Semi-Auto	Semi-Auto
	Synthesis	Manual	Manual	Semi-Auto	Semi-Auto
Package	Spice Chip/Pack.				
	P&R Chip/Pack.				

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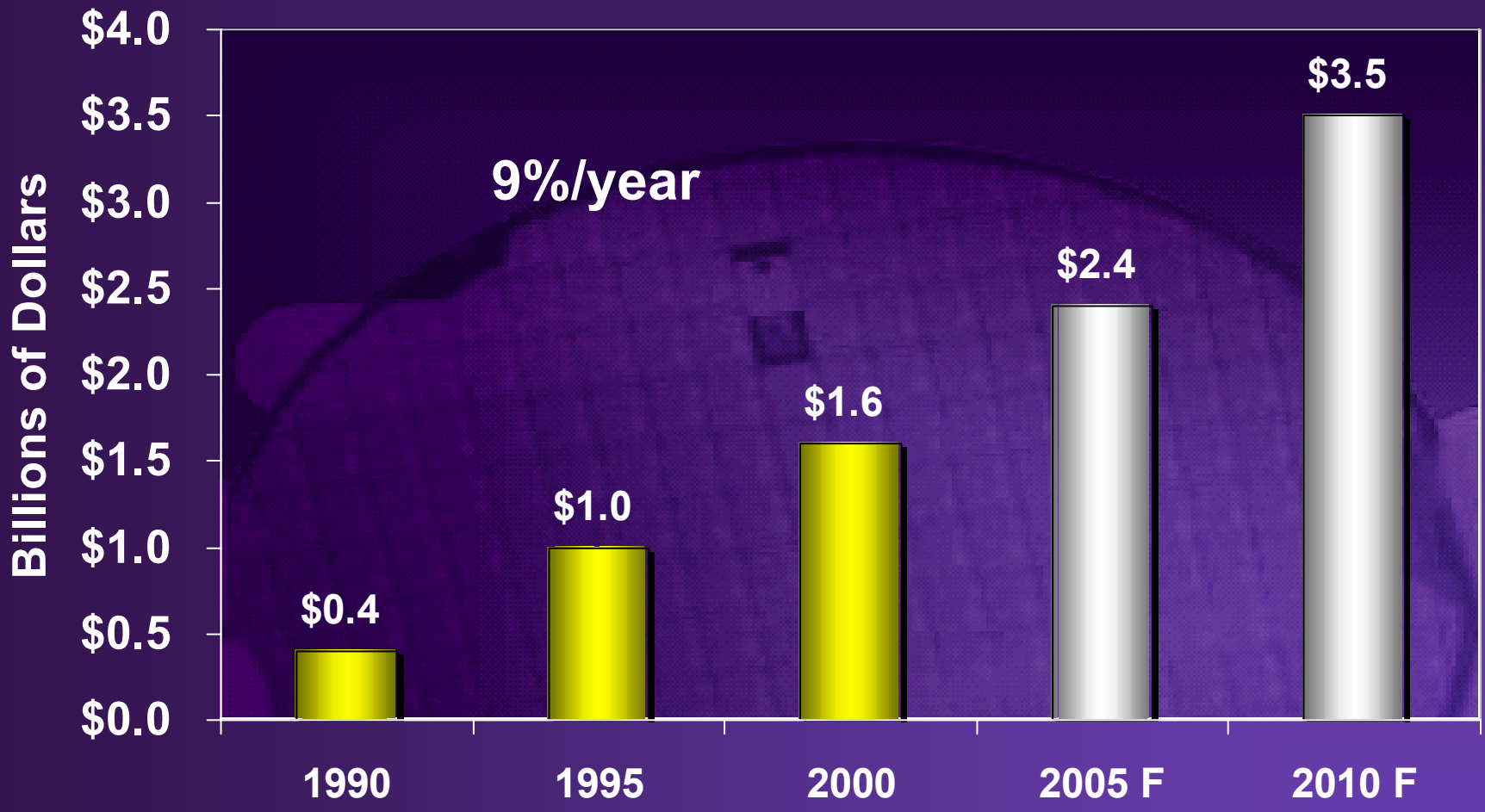
Wafer Fabs Keep Getting Pricier



Source: IC Insights, April 2003

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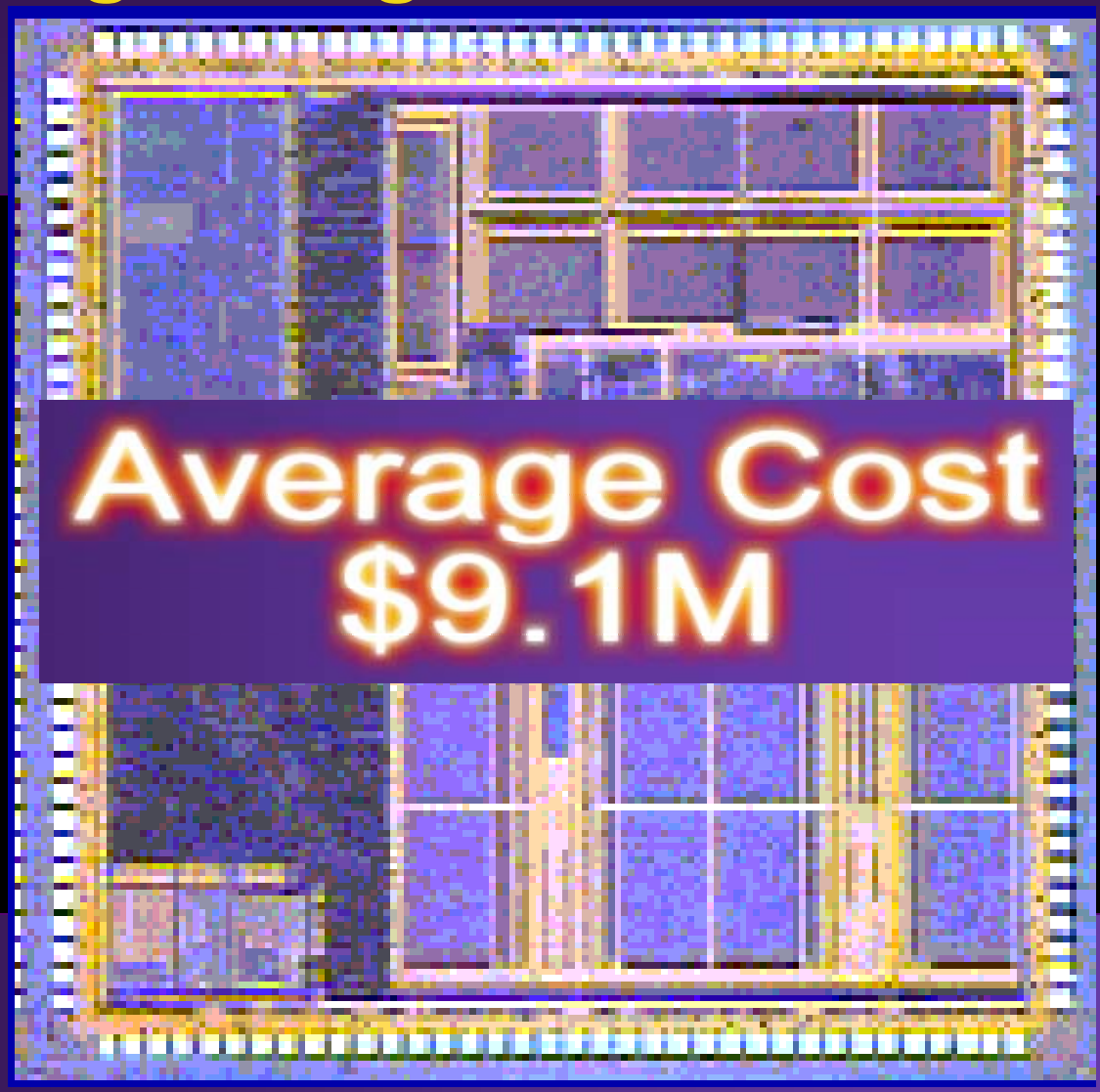
Resulting in large NRE Costs



Source: IBS

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Alliance between
STMicroelectronics
Philips
and Motorola

Crolles2 Alliance 300mm Pilot Line

Henri-Alain Rault
General Manager Philips Crolles SAS

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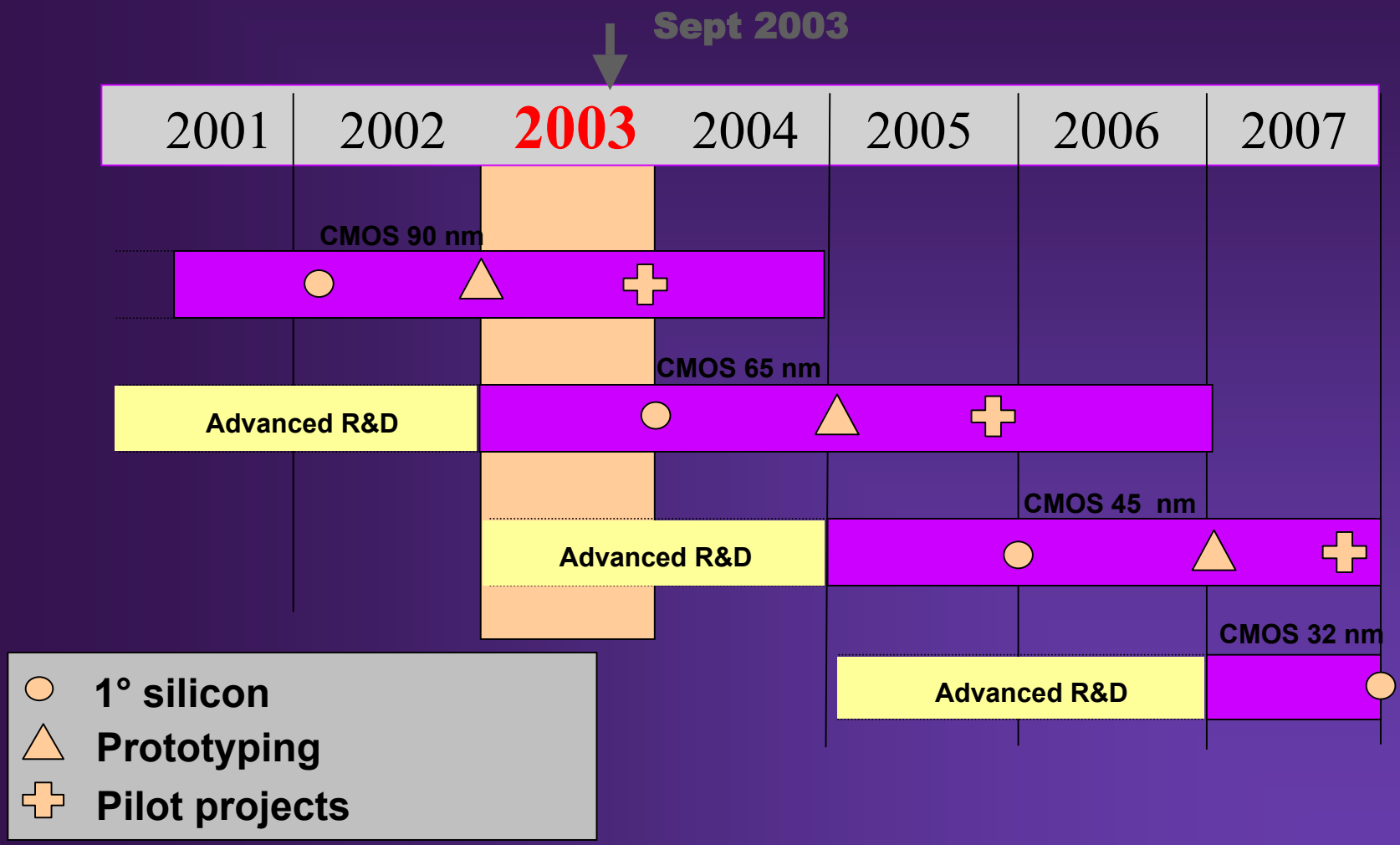
CMOS Technology in Crolles2



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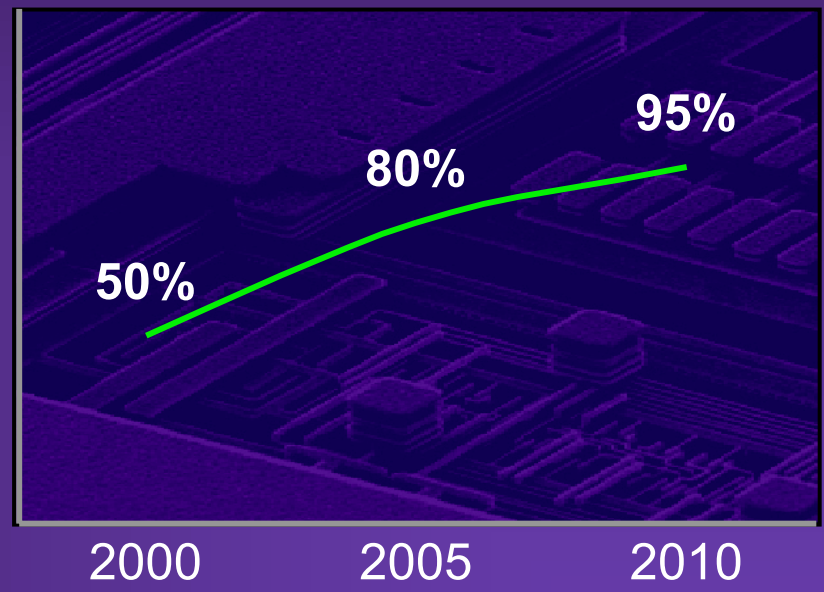
Solution: Increasing Volumes, Increasing Use of IP

Volume (2002)	M Units
Cable modem	111
Digital Cable Set-Top Boxes	48
xDSL modems/Line card	67
Cellular Phones (only 2.5G, 3G)	25
Satellite Set-Top Boxes	23
WLAN 802.11b	15
Video surveillance	15
Digital Still Cameras	10
Laser Printers	8
Auto display / dashboard control	6
Digital Camcorders	5
Auto Navigation	4
Digital TV Sets	4
Digital Copiers	2
WLAN 802.11a	2

IP Blocks as % of an SoC



Source: Dataquest, 2000

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Agenda

- A glimpse backward: models that have worked in the past
  - The PC Paradigm
  - Standards
  - Examples
- A glimpse forward:
  - More complex IP
  - Platforms
- Conclusions

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What Works

Semiconductors	$141B
Micros, DSP	$43.4B
Memory	$30.8B
ASIC, ASSP	$37.8B
Analog, Discrete	$28.0B

Standards enable Large Volumes

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PCs Scalable by Sticking to Standards

Name	IBM PC AT
Year	1984
CPU	Intel 80286
I/O Ports	six-16 bit & two 8-bit ISA
OS	MS DOS
Graphic Modes	EGA: 640x350

Name	Dell Inspiron 5150
Year	2003
CPU	Intel Pentium4
I/O Ports	IEEE 1394, USB 2.0, 10/100 Ethernet
OS	Windows XP
Graphic Modes	SXGA+

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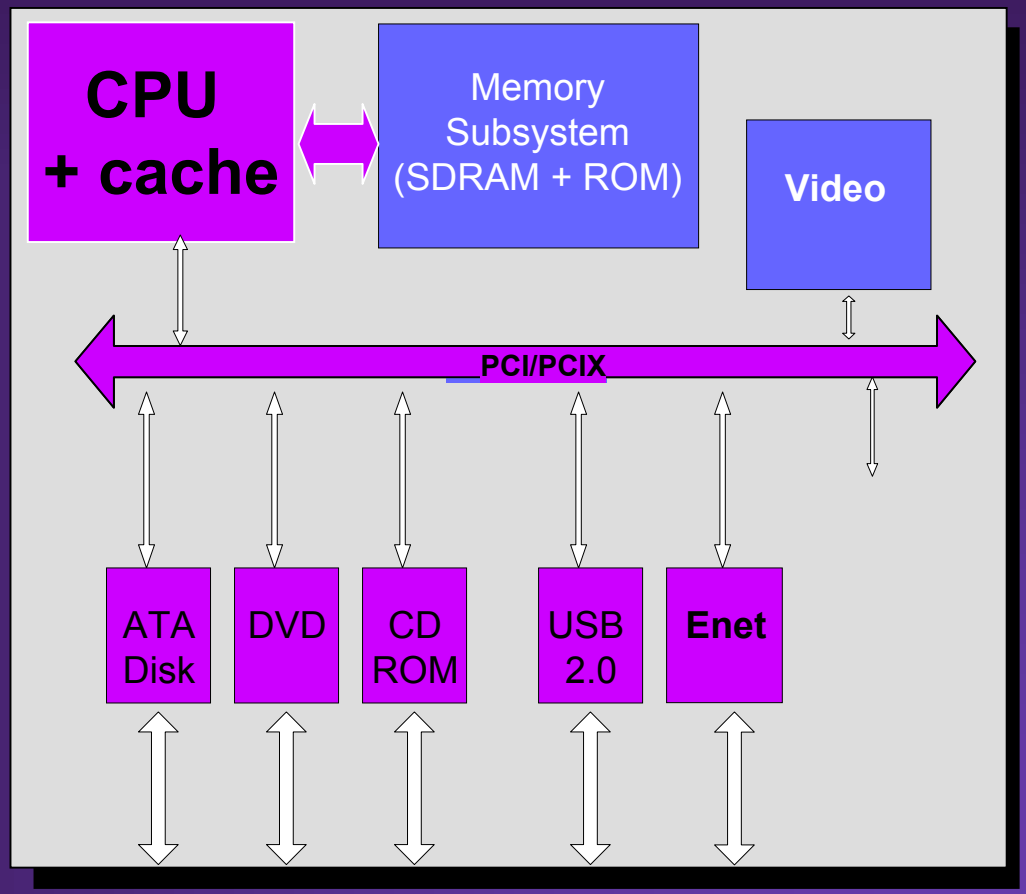
What's in the Box?



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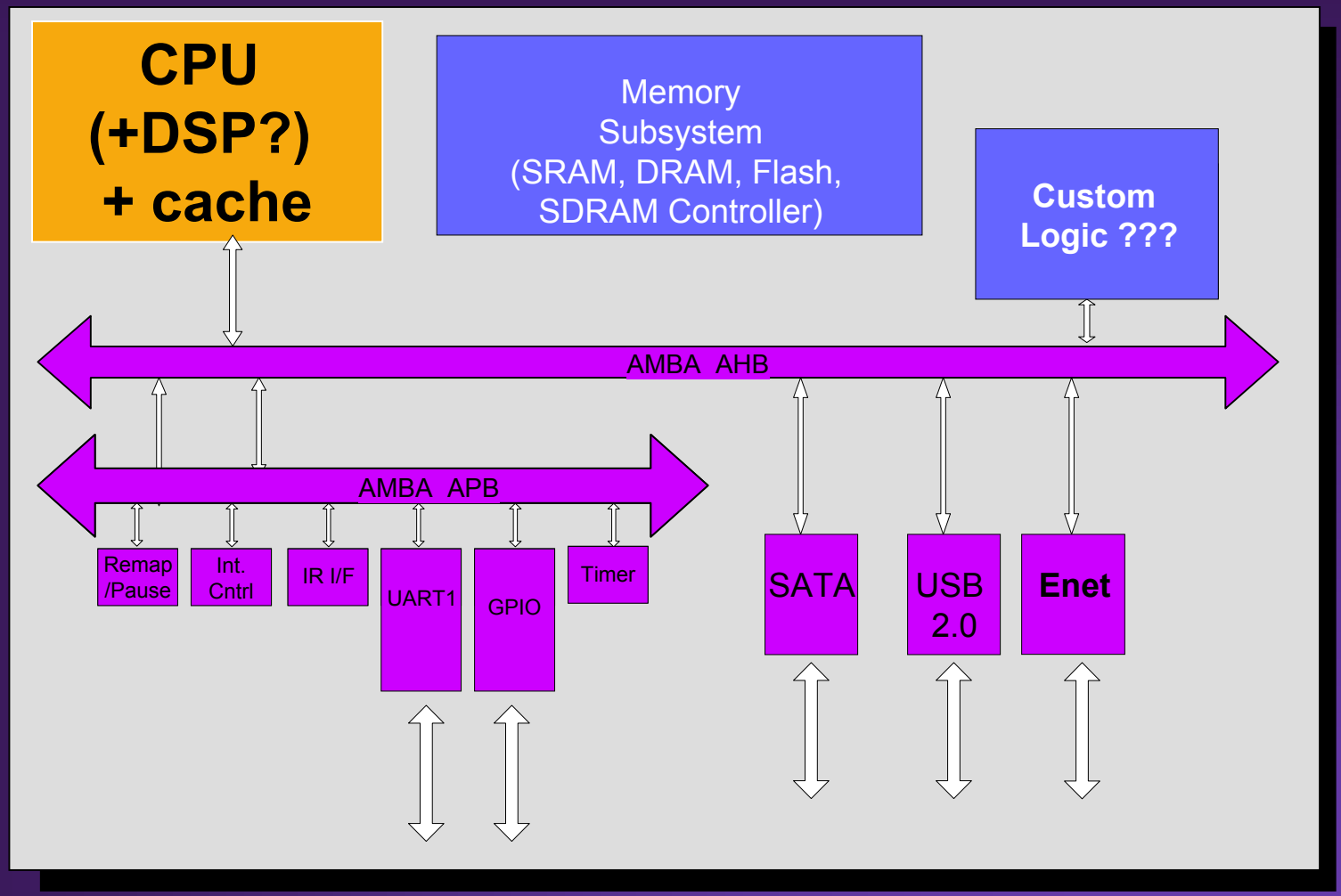
What's in an SoC?



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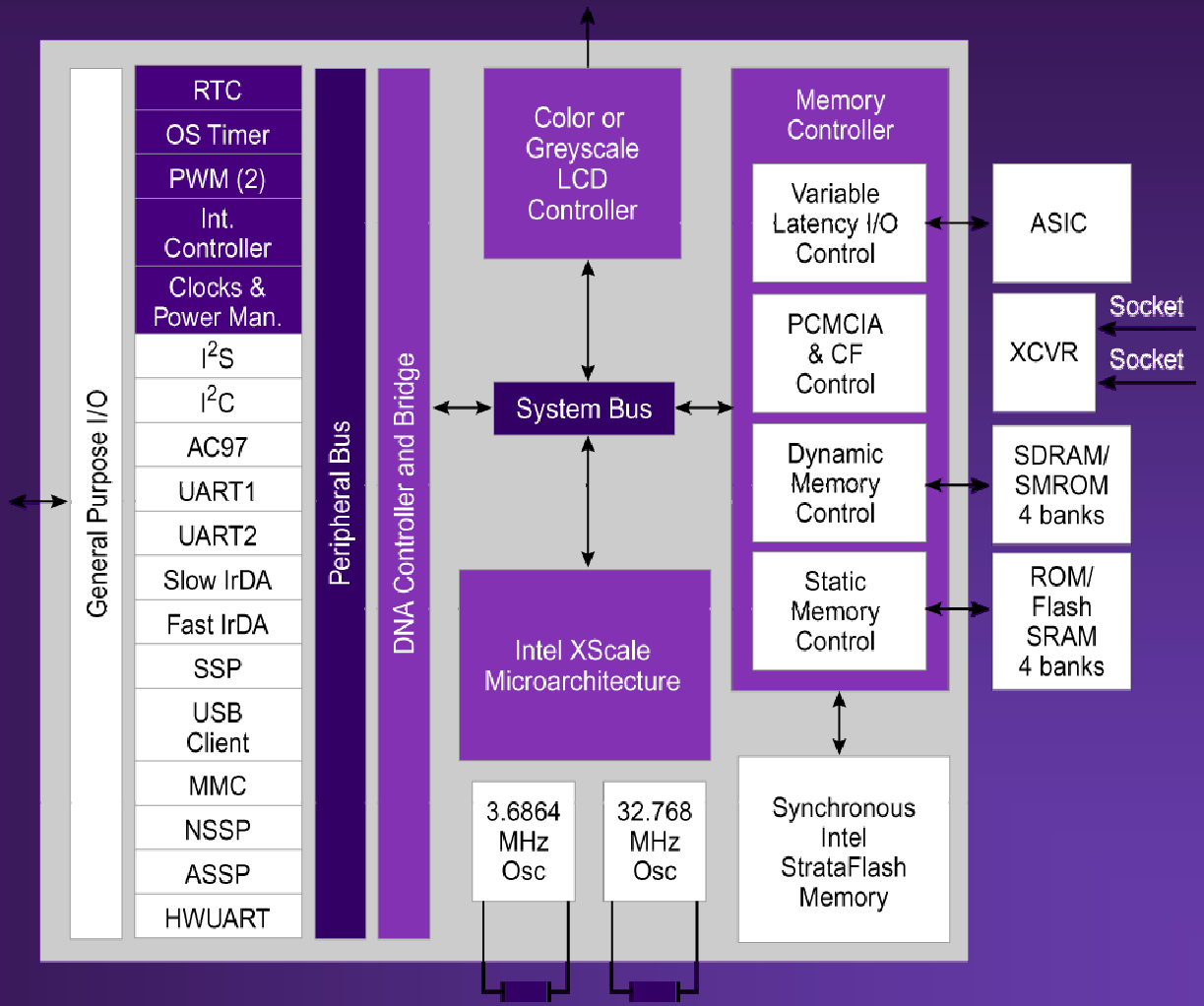
Intel's XScale Architecture



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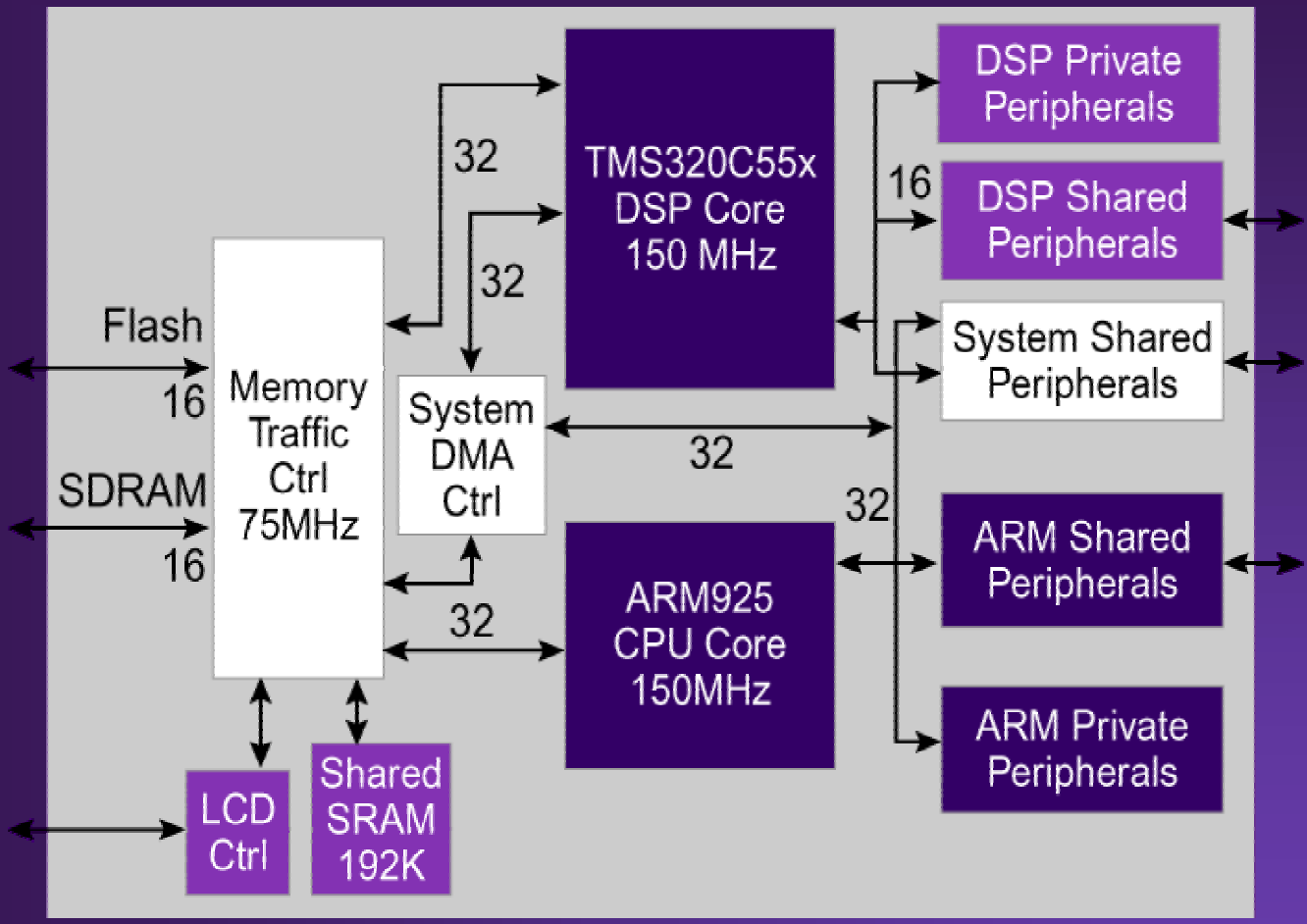
Source: Microprocessor Report, Dec.. 2002

TI OMAP 5910



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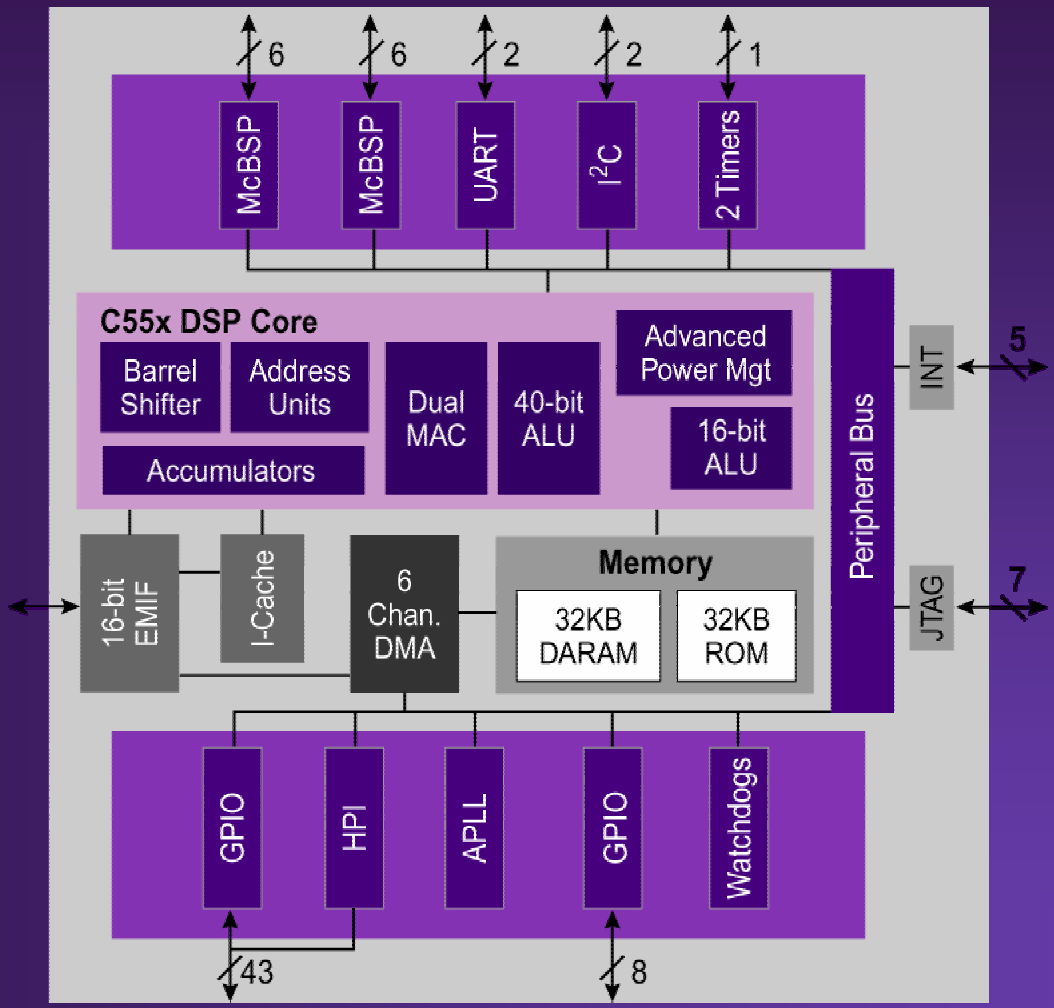
Source: Microprocessor Report, Sept.. 2002

TI DSP C5501



Source: Microprocessor Report, Jan. 2003

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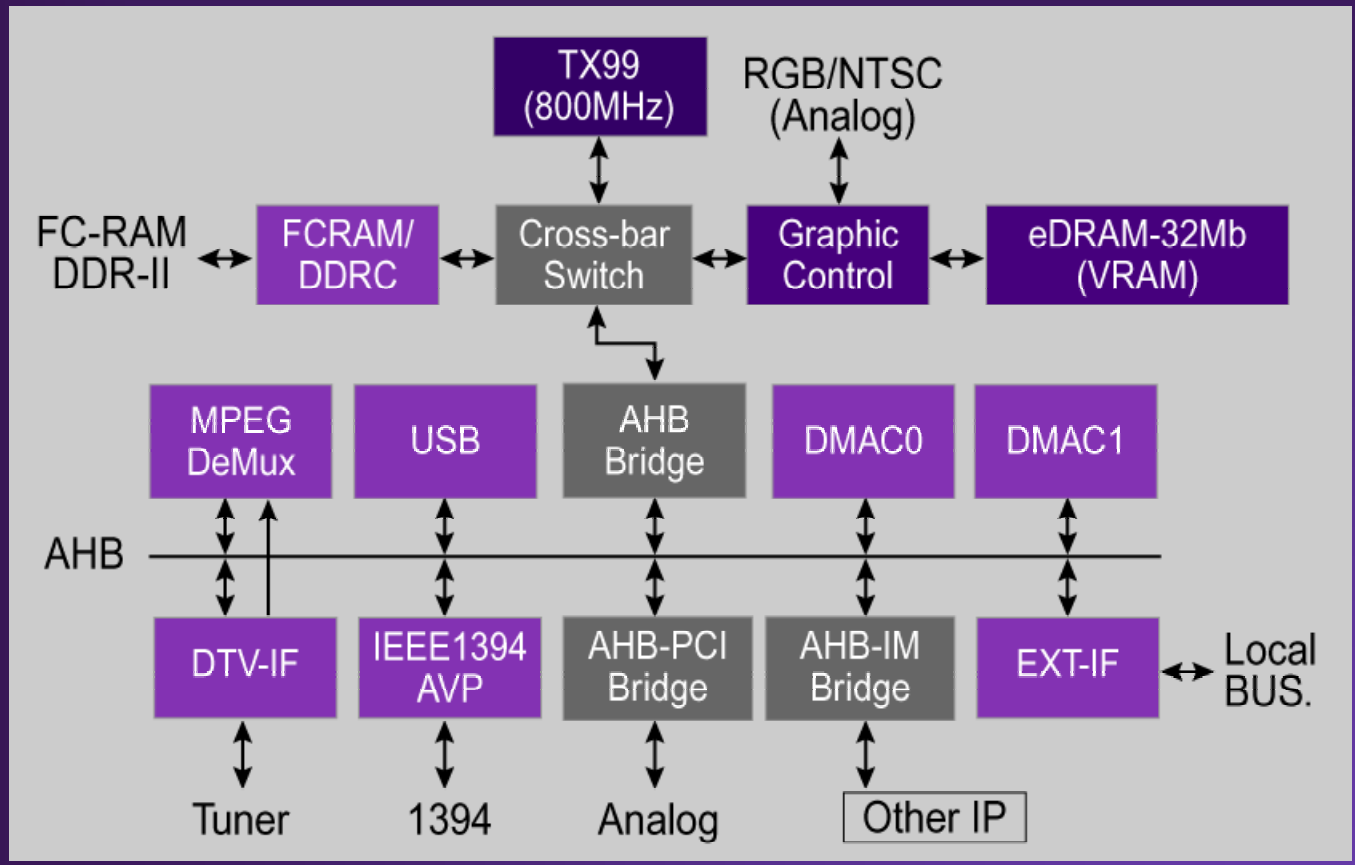
Toshiba MIPs-based SoC



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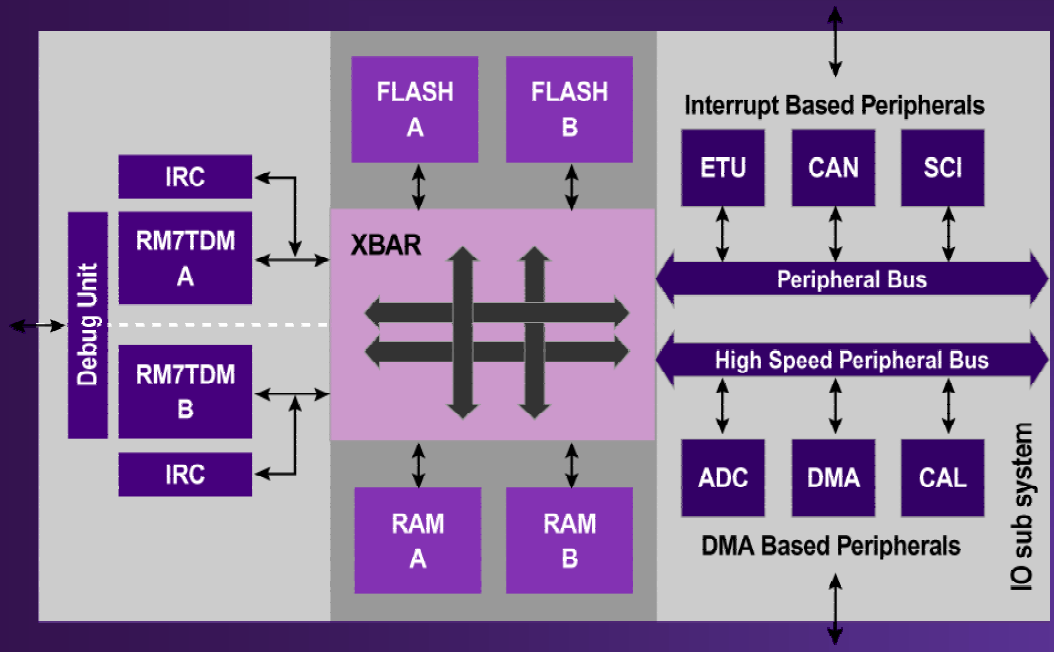
Source: Microprocessor Report, Nov.2002

SoC Automotive Transmission Controller



- Transmission controller
- CPU: ST10
- On-chip RAM
- Embedded 4Mbits Flash
- Transmission controller
- CPU: ST10
- On-chip RAM
- Embedded 4Mbits Flash
- Dual ARM architecture
- Embedded Flash
- Internal cross bar switch

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Convergence of Hardware Architectures

- Processors
  - ARM and DSP
- Memory
  - Over half the chip
- IO
  - Driven by (a few) standards
  - Sometimes processor-based (recursive)

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Convergence of IP Market

- Processors
  - ARM and MIPS
  - DSP not yet sorted out
- Memory
  - Virage, Artisan, Mosys
- IO
  - Synopsys and ARC and Mentor

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Critical IP Aspects

Poor IP design makes:

- Development time and performance unpredictable
- Integration effort exponential with the # of blocks

Good IP design makes:

- Development time and performance predictable
- Integration effort linear with the # of blocks

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Critical IP Aspects

- Functional Correctness – Complex design
  - Across configuration space
  - In any design context
- Interoperability - Standards
  - Plug and Play in your design
- Configuration/Integration
  - Consistent, legal configuration
  - Tool flows supported cleanly
  - Complete deliverables

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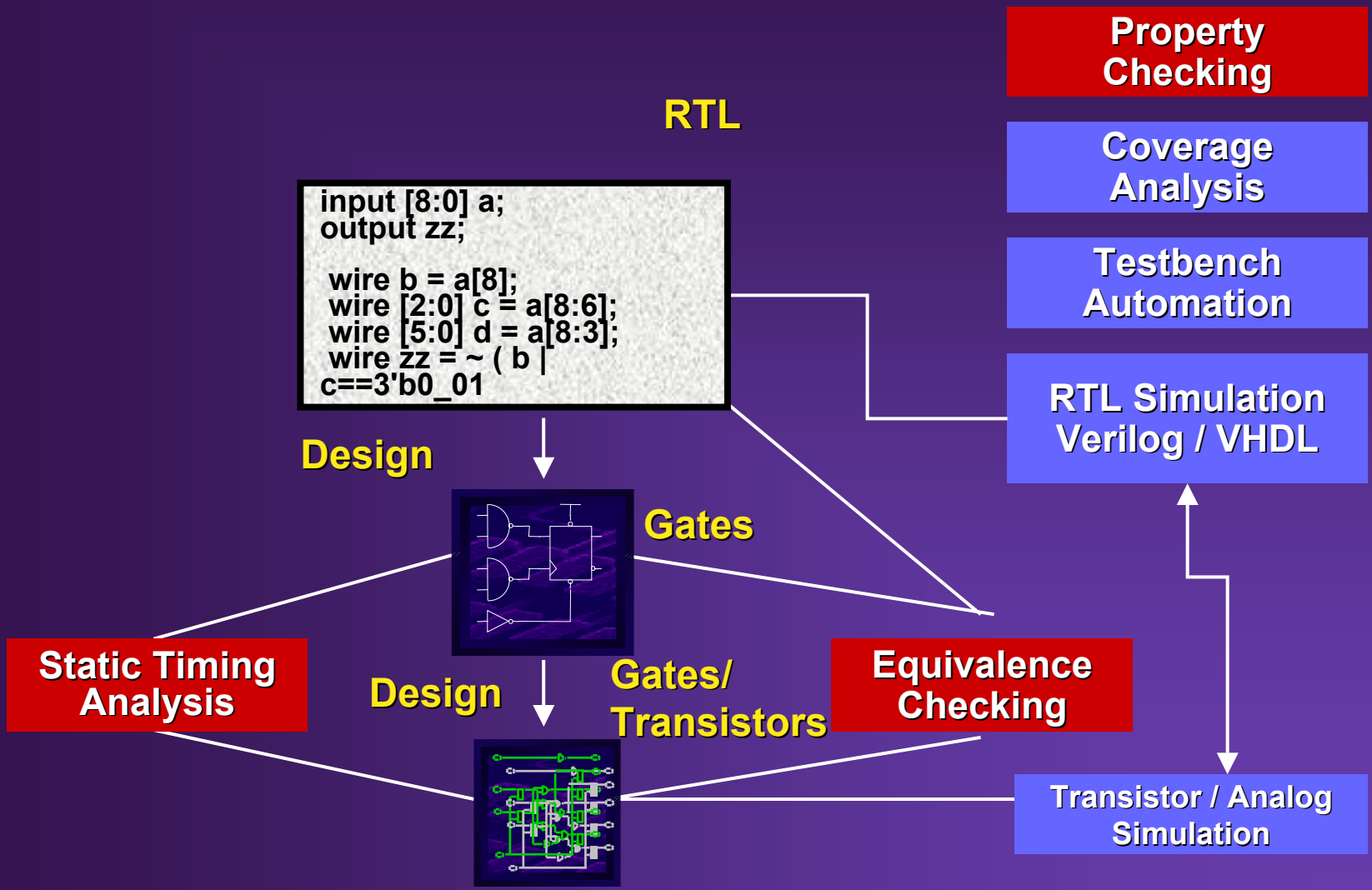
Functional Verification Includes Simulation and Formal Techniques



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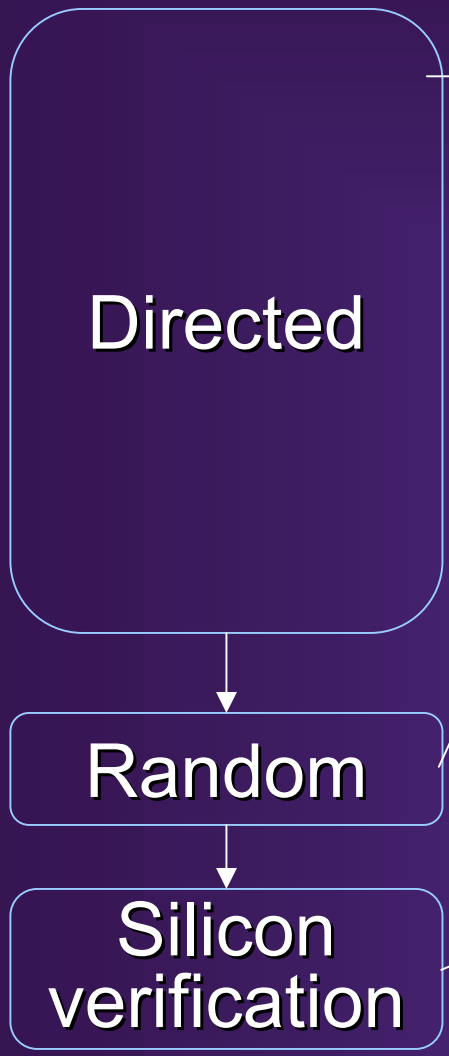
Typical Verification Methodology



- limited to covering the test cases that have been identified

- Ad-on to directed test environment
- Limited to randomizing BFM command stream
- Unable to adequately emulate real-world stimulus and automatically check response resulting in major holes in random test coverage

- limited to a small subset of possible target systems and drivers
- debug cycle is extremely long

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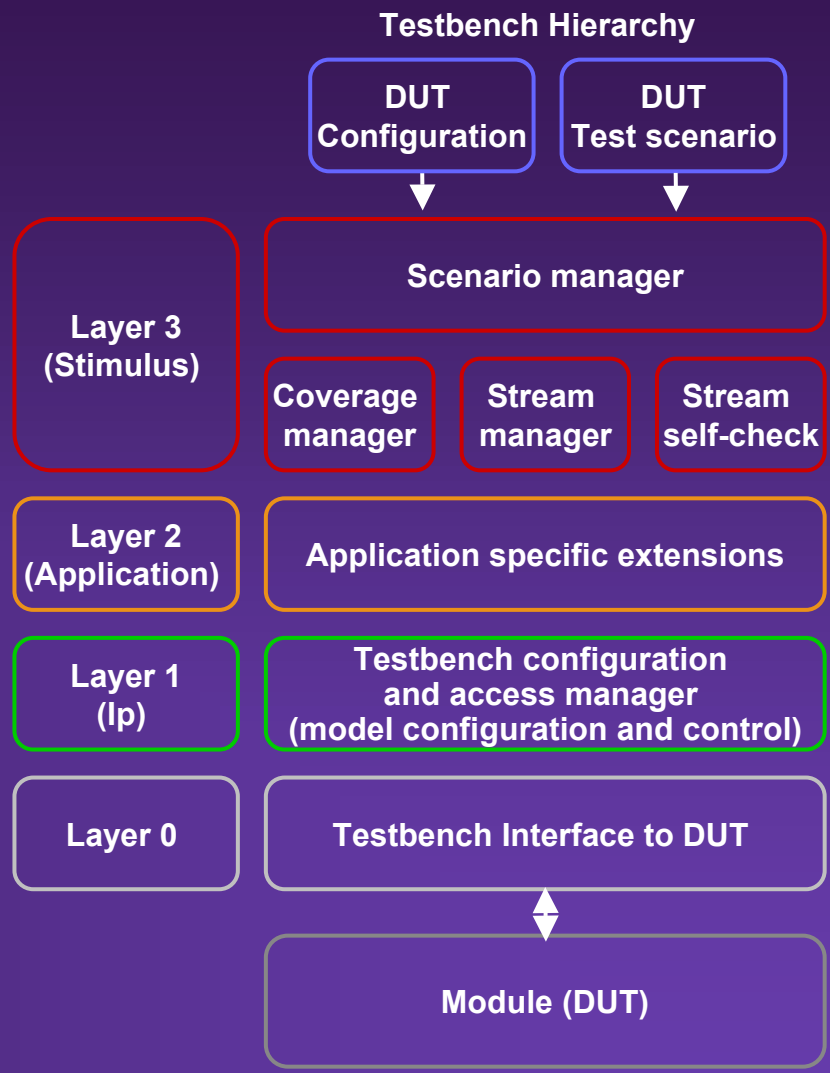
“Smart” Verification Platform

- “Smart” test environment
  - Speeds up test authoring
- Self-checking architecture
- Reuse from sub-system to system level testing
- Reuse for other projects
- Resilient to design changes
  - e.g. only need layer-1 modifications
- Quantitative quality metrics
  - Code coverage
  - Functional coverage



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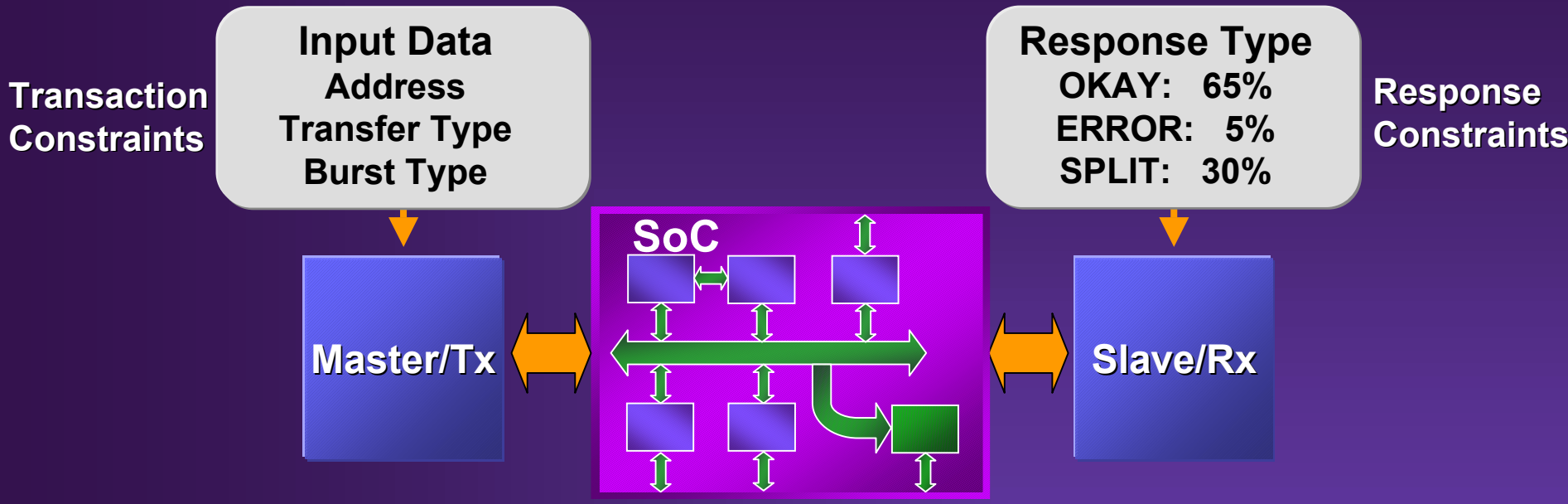
Constrained Random Finds More Bugs



- Many test scenarios with few commands
- Finds complex sequences impossible with directed test

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Optimal CRV Is Essential Because…

- … it's the only way to find bugs that occur exclusively under complex combinations of
  - Bus traffic
  - Configurations
  - Parameters
  - Timing windows
- ... it is humanly impossible to think of all the cases CRV generates!!!

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Experience Shows That It Works

- 3 “mature” cores reverified
  - In production from 6 months-3 years
  - Passed all compliance testing
  - Scores of tapeouts
- Optimal CRV found average 20-30 bugs
- 15-20% severe, no workaround

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IP Products

Basic Library	Verification Library	Standard Cores	Star IP

■ Data path
■ Memory
■ OCB/AMBA
■ Building Blocks
■ DW Verification Library
	■ Ver. Suites
	  ■ AMBA
	  ■ PCI, PCI-X
	  ■ USB OTG …
	■ Memory Models
		■ USB1.0, 2.0, ..
		■ PCI, PCI-X, ...
		■ Ethernet 10/100,..
		■ Bluetooth
		■ USB PHY…
			■ MIPS 4KE
			■ TriCore1
			■ C166S
			■ V850E
			■ PPC 440
			■ …

■ Complete SoC infrastructure IP ■ Improved QoR ■ Smart Verification	■ Smart Verification ■ Standard protocol verification ■ Verification farms	■ Connectivity IP ■ Interoperability ■ Time to market	■ Partner licenses ■ Synopsys supports

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An SoC Perspective On Platform-based Design

- A Platform
  - An essentially defined architecture*: increased complexity & cost
- VSIA Established DWG On Platform-based Design
  - Platform-based design : “an integration-oriented approach emphasizing systematic reuse, for developing complex products based on platforms and compatible hardware and software VCs, to reduce development risks, costs, and TTM”
  - Observation: bottom-up to date by chip makers intent on reuse

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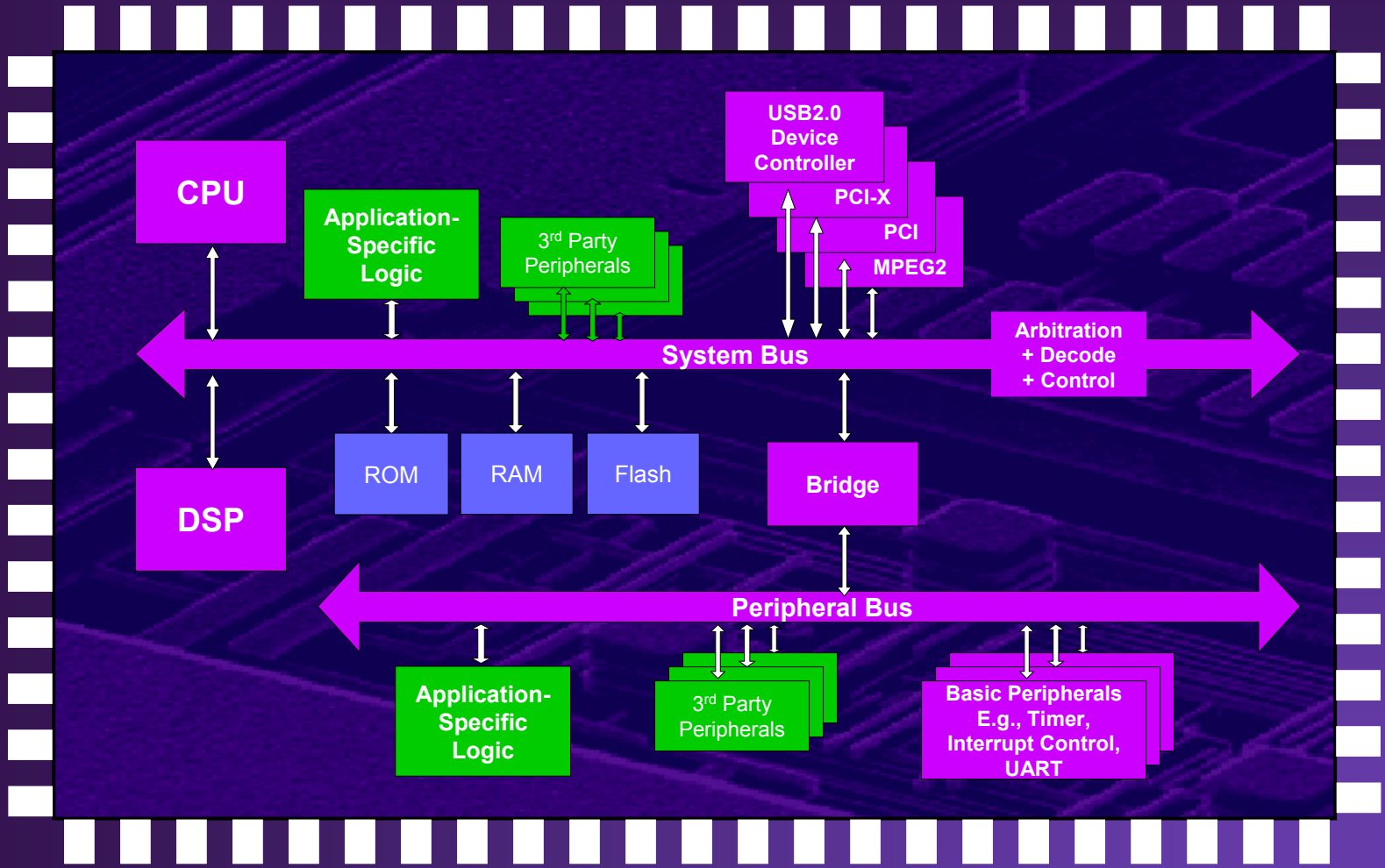
*Gary Smith

From IP to Platforms



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The Future

- IP reuse up to 99%
- IP complexity comparable to SoC
- Standards are key
- Verification IP
- Platforms
- More functionality in SW

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Economics: Standards-based IP

- Initial development
  - Understand the standard
  - Functional spec, architecture design
  - Implementation, verification, flow testing
  - Certification (test chips, boards, lab, …)
  - Documentation
  - Packaging & release

The typical core development project today takes roughly 5-20 person years to complete

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Economics: Standards-based IP

- Maintenance
  - Bugs / enhancements
  - Track standard
  - Add new interfaces
    - -> Initial development
  - Run regressions

The typical core maintenance today runs at roughly 1-2 person years per year

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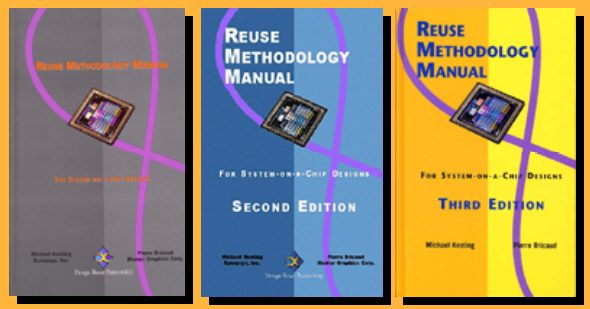
Strong Forces for Consolidation In IP Providers

- Small vendors are just too high risk
- Multiple vendors on one chip brings multiple challenges



Elements for greatly reducing risk:

- Choose widely used, trusted cores
- Inspect reuse methodology
- Insist on advanced verification technology

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IP Providers

Rank	Company	2001 ($M)	2002 ($M)	Growth	Share	Cumulative Share
1	ARM	168.0	184.9	10%	20%	20%
2	Rambus	107.3	97.4	-9%	10%	30%
3	Synopsys *	45.0	73.2	63%	8%	38%
4	TTP Com	39.5	58.0	47%	6%	44%
5	ParthusCeva *	40.9	51.2	25%	5%	50%
6	Virage Logic	34.8	47.5	36%	5%	55%
7	Artisan	27.8	43.7	57%	5%	60%
8	MIPS Technologies	70.2	43.1	-39%	5%	64%
9	Mentor Graphics	30.4	25.7	-15%	3%	67%
10	Monolithic System Technology	9.5	24.9	162%	3%	70%
11	ARC International	16.5	17.7	7%	2%	71%
12	LogicVision	17.3	15.6	-10%	2%	73%
13	Nurlogic	15.1	15.4	2%	2%	75%
14	LEDA Systems	16.2	15.3	-5%	2%	76%
15	Imagination Technologies	11.4	15.3	35%	2%	78%
16	Newlogic Technologies	7.0	15.0	114%	2%	80%
17	Tensilica	21.1	12.8	-40%	1%	81%
18	Cadence Design Foundry	15.5	12.4	-20%	1%	82%
19	Virtual Silicon	13.7	10.1	-26%	1%	83%
20	Sarnoff	7.0	9.6	38%	1%	84%
	Total Top 20	**714.0**	**788.8**	**10%**	**84%**	**84%**
	Others *	177.4	145.0	-18%	16%	100%
	Total	**891.5**	**933.8**	**5%**	**100%**	**100%**

Source Gartner Dataquest April 2003

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IP Market Segments and Growth

	2001	2002	Growth
Microprocessor and DSP Cores	301.4	273.4	-9%
Platforms	98.7	127.2	29%
Signal Processing	33.3	36.9	11%
Networking	44.4	42.6	-4%
Block Libraries	54.3	54.2	0%
Bus Interfaces	30.9	31.6	2%
Chip Infrastructure and Test IP	25.3	24.2	-4%
Other	73.2	85.6	17%
Memory	64.6	93.8	45%
Physical Libraries	32.9	39.5	20%
Analog Mixed Signal	25.3	27.3	8%
Rambus	107.3	97.4	-9%
Total IP	891.5	933.8	5%

Source: DataQuest April 2003

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Summary

- IP diversity matters
  - It is kept in check by standards
  - IP needs to work together – platforms
- IP vendor size matters
  - IP needs to be certified by the vendor
  - The user certifies the vendor
- Consolidation is unavoidable

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Design

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